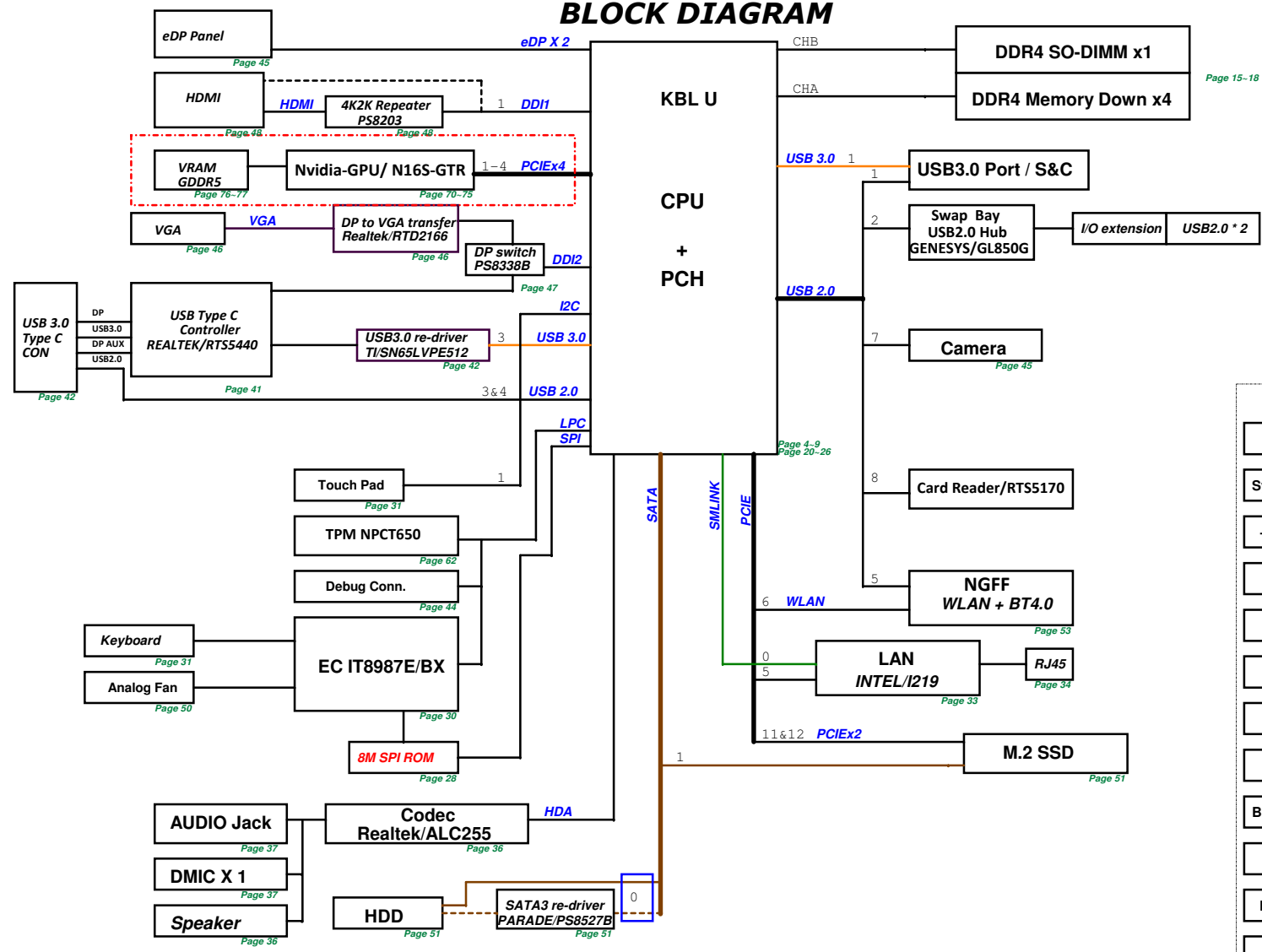


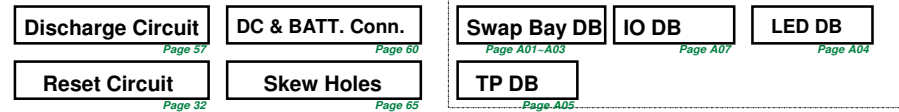
- 01. Block Diagram
- 02. System Setting
- 03. CPU(1) \_DDI/eDP
- 04. CPU(2) \_DDR4
- 05. CPU(3) \_+VCCCORE
- 06. CPU(4) \_+VCCGT
- 07. CPU(5) \_+VDDQ/IO/SA
- 08. CPU(6) \_CPU GND
- 09. CPU(7) \_CFG/RSVD
- 15. DDR4(0) \_Termination
- 16. DDR4(1) \_Memory Down
- 17. DDR4(2) \_SO-DIMM1
- 18. DDR4(3) \_CA/DQ Voltage
- 20. PCH(1) \_SMB,LPC
- 21. PCH(2) \_LPS5,ISH
- 22. PCH(3) \_HDA,SDIO
- 23. PCH(4) \_PCIE,SATA,USB,SSIC
- 24. PCH(5) \_CLK,RTC,HDA,SDIO
- 25. PCH(6) \_SYS PWR
- 26. PCH(7) \_POWER
- 28. PCH(8) \_SPI,SMB
- 30. EC \_IT8987E/BX
- 31. TP / Keyboard
- 32. RST \_Reset Circuit
- 33. INTEL LAN \_I219
- 34. RJ45
- 36. AUDIO \_ALC255
- 37. AUDIO \_COMBO JACK
- 40. Card Reader-RTS5229
- 44. BUG \_Debug
- 45. eDP \_output
- 46. CRT RTD2166
- 47. Display Port Switch
- 48. TV(1) \_HDMI
- 50. THERMAL / FAN
- 51. SATA HDD/ SSD
- 52. USB JACK
- 53. NGFF \_WLAN/ WiGig
- 56. LED
- 57. Discharge
- 60. DC-IN/ Batt connector
- 61. Touch Panel
- 62. TPM
- 65. ME \_CONN,Skew Hole
- 66. BRD Conn
- 67. MLB to IO
- 68. BYPASS EC SEQUENCE
- 70. VGA-PCIE
- 71. \_VGA-N16P-GT FRAME BUFFER GDDR5
- 72. \_VGA \_RGB,XTAL GDDR5
- 73. \_VGA \_LVDS \_HDMI GDDR5
- 74. \_VGA \_GPIO,STRAP GDDR5
- 75. \_VGA \_Power,GND GDDR5
- 76. \_VGA \_CHA VRAM GDDR5
- 77. \_VGA \_CHB VRAM GDDR5
- 80. \_POWER \_VCORE for U22
- 81. \_POWER \_SYSTEM
- 82. \_POWER \_+1.0VSUS & 2.5V
- 83. \_POWER \_DDR & VTT \_DSC
- 84. \_POWER \_+1.8VSUS
- 85. \_POWER \_+1.5VS \_VGA
- 86. \_POWER \_+1.05VS \_VGA
- 87. \_POWER \_+VGA \_VCORE
- 88. \_POWER \_CHARGER
- 89. \_POWER \_AC\_PD Input
- 90. \_POWER \_DETECT
- 91. \_POWER \_LOAD SWITCH
- 92. \_POWER \_PROTECT
- 93. \_POWER \_SIGNAL
- 94. \_POWER \_FLOWCHART
- A01. P4 \_Swap Bay
- A02. P4 \_Smart card reader
- A03. P4 \_IO DB
- A04. P4 \_LED DB
- A05. P4 \_TP Button DB
- A06. P4 \_KB LED DB
- A07. P4 \_IO DB

# P2 Kaby Lake U (2+2) Rev1.0

## BLOCK DIAGRAM



### D.B.



Function Remove List:

- 1. Remove WIGIG
- 2. Remove NFC
- 3. Remove Touch Panel
- 4. Remove Finger Print
- 5. Remove G-Sencor
- 6. IO Board remove Smart Card Reader and one Port USB2

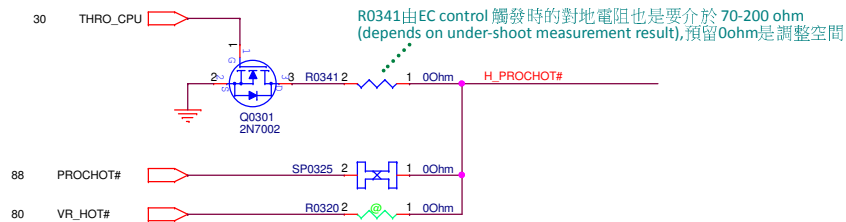
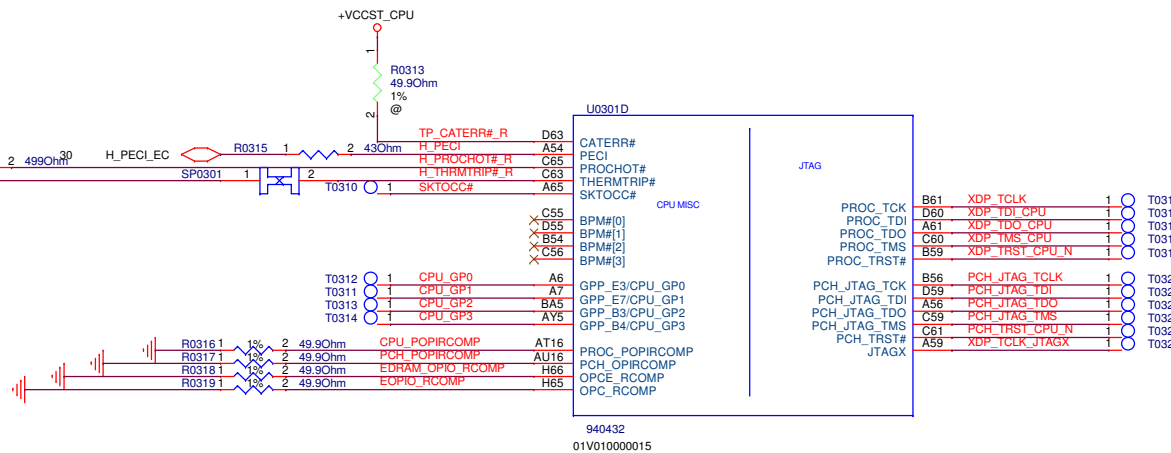
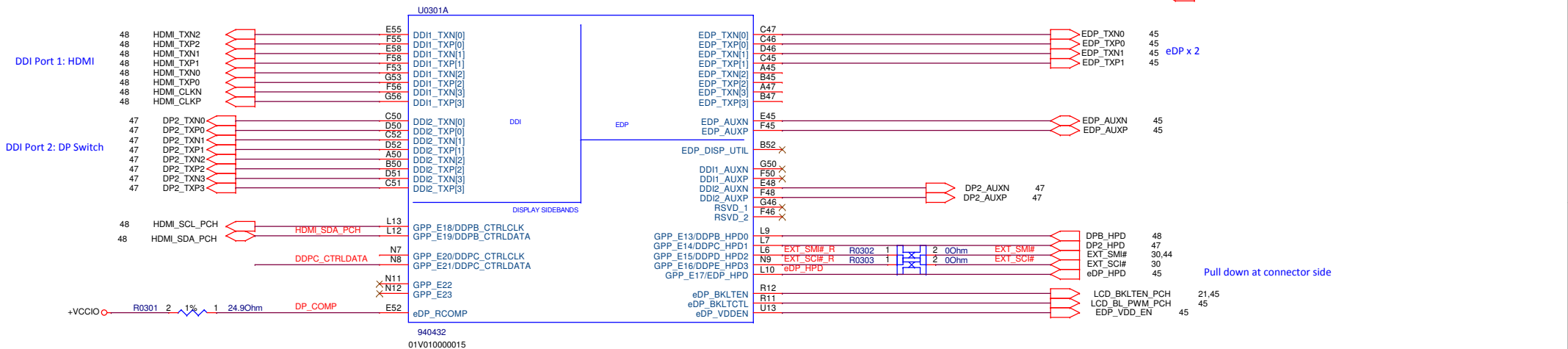
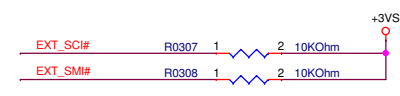
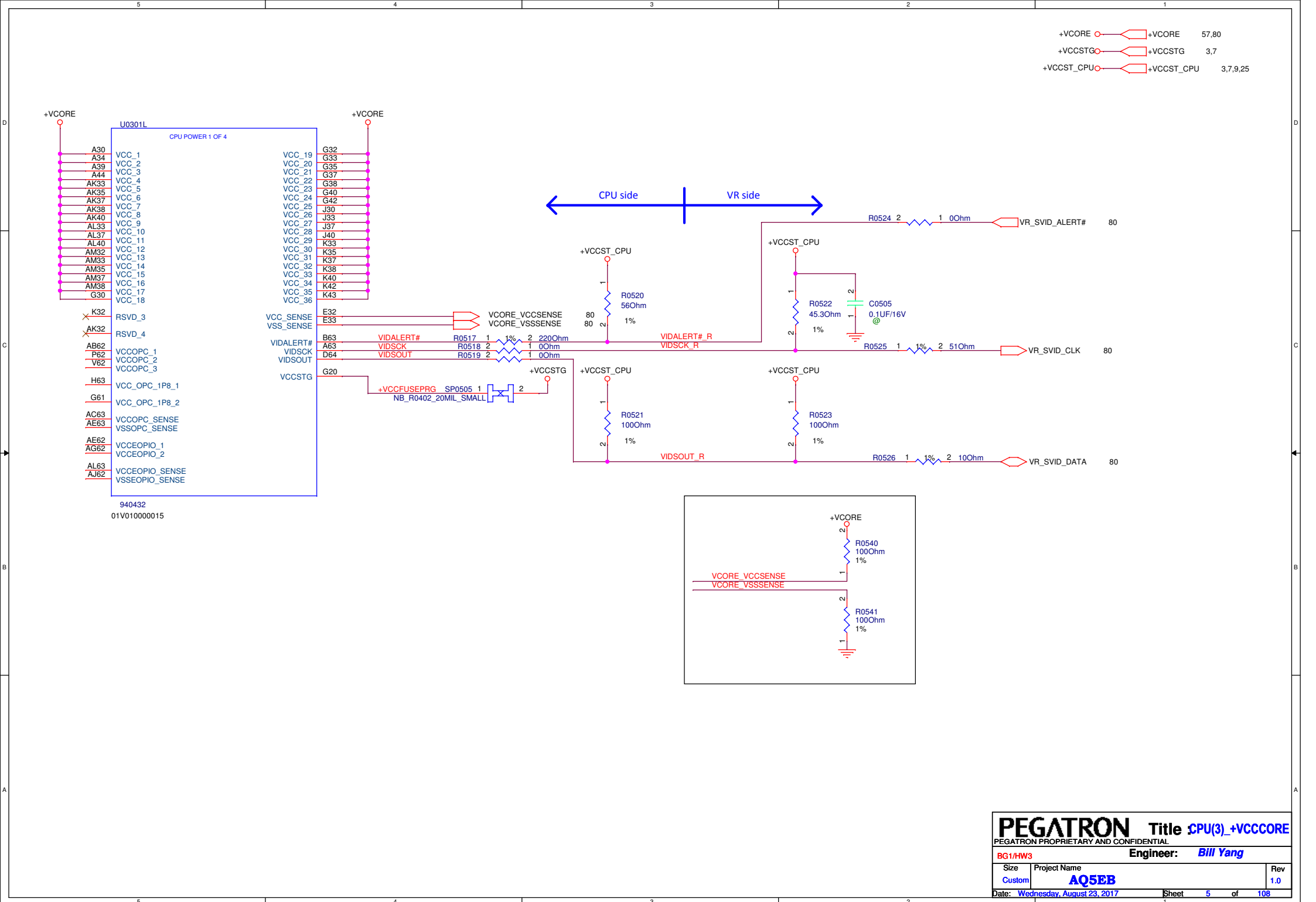


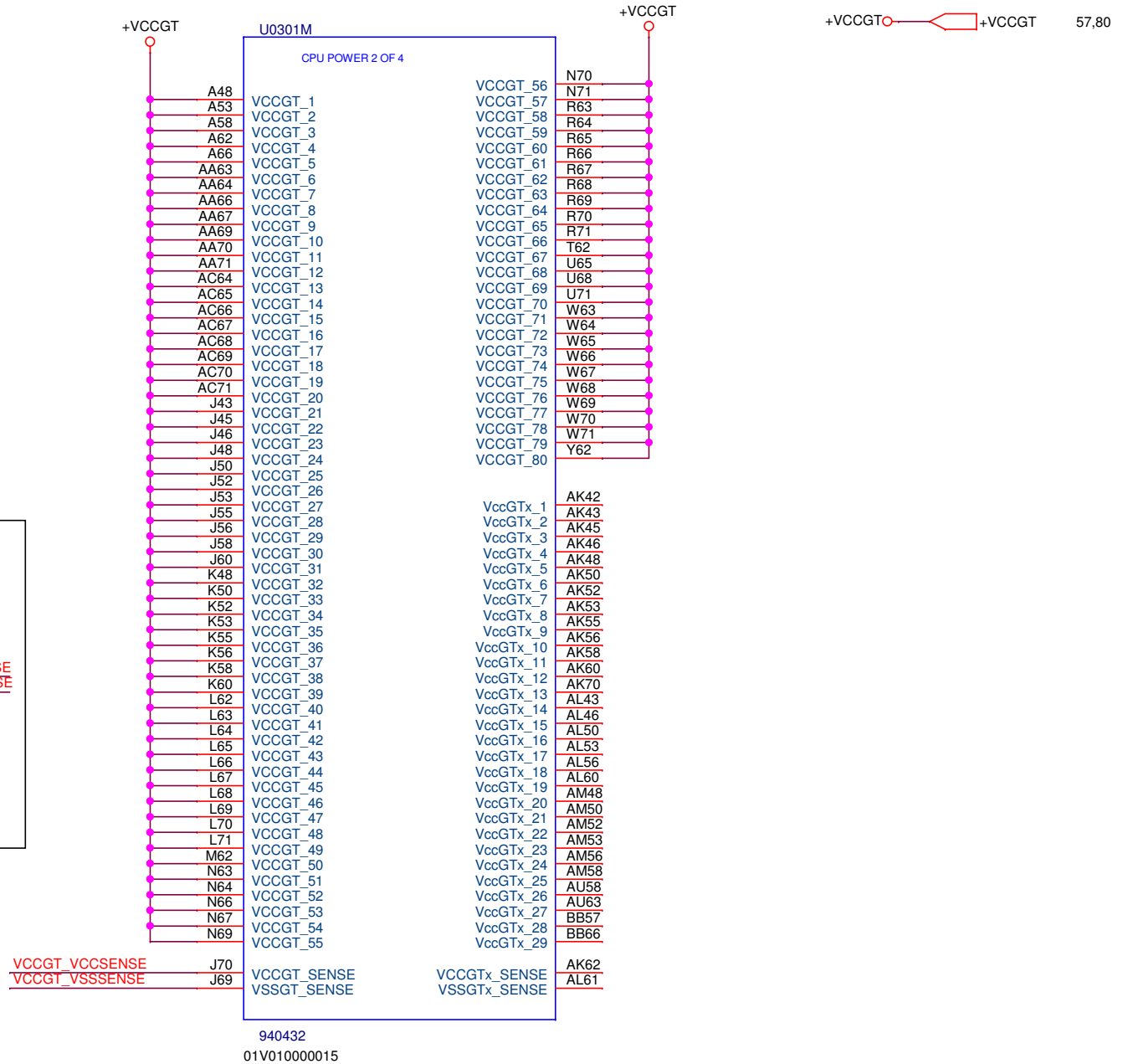
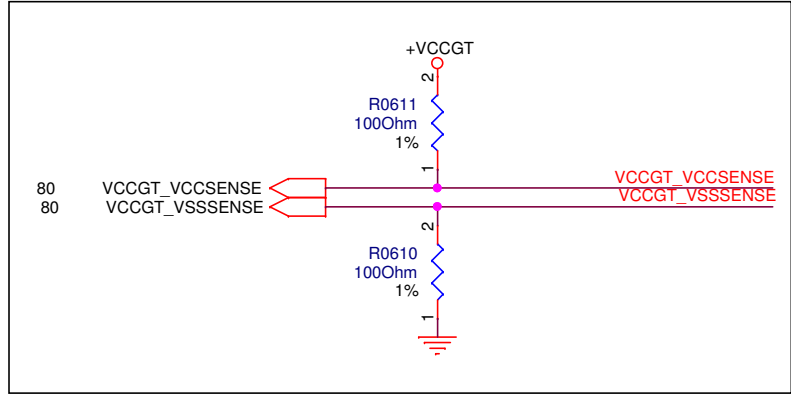
Table 5-10. DDI Disabling and Termination Guidelines

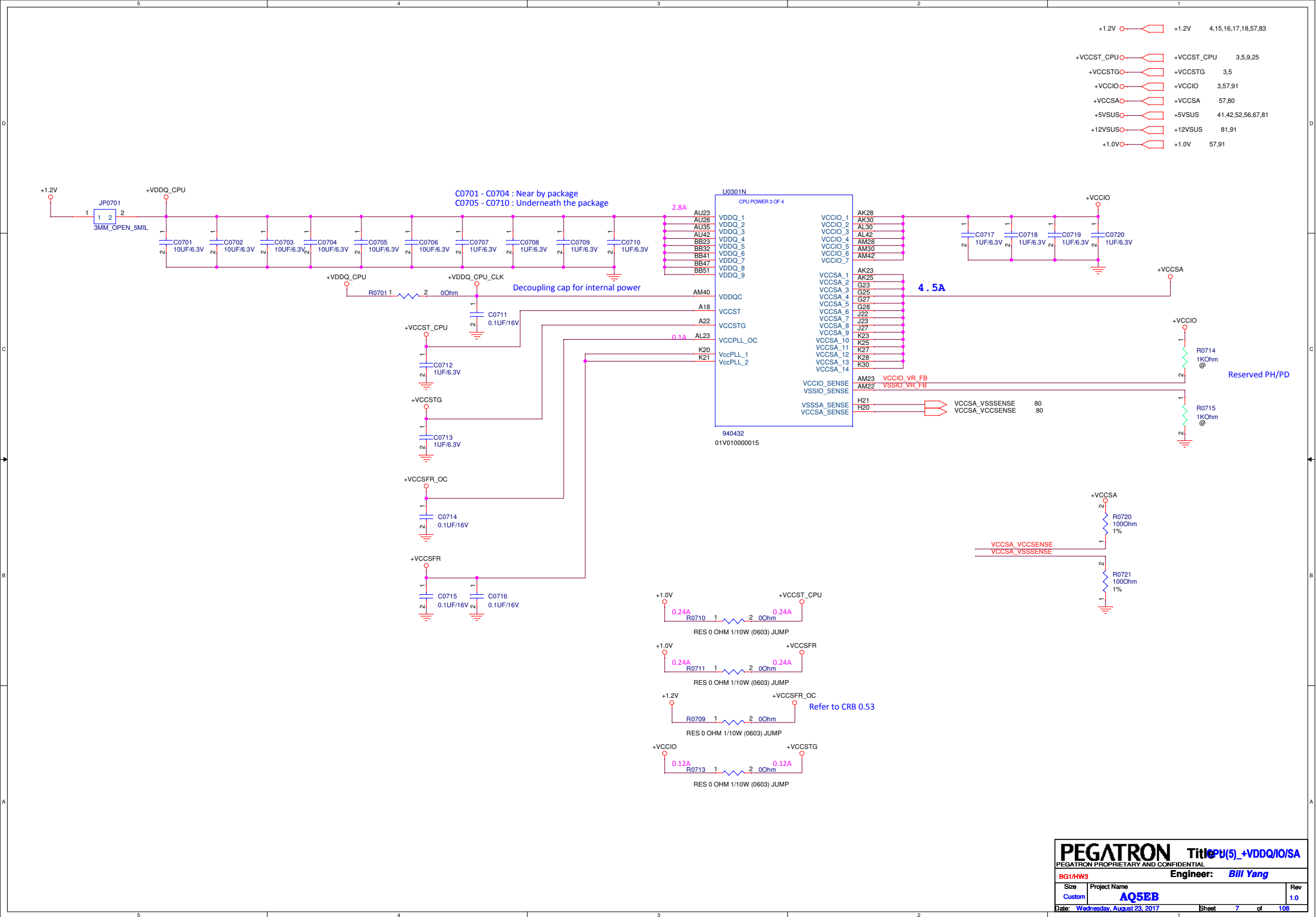
Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k W ±5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k W ±5% resistor	No Connect

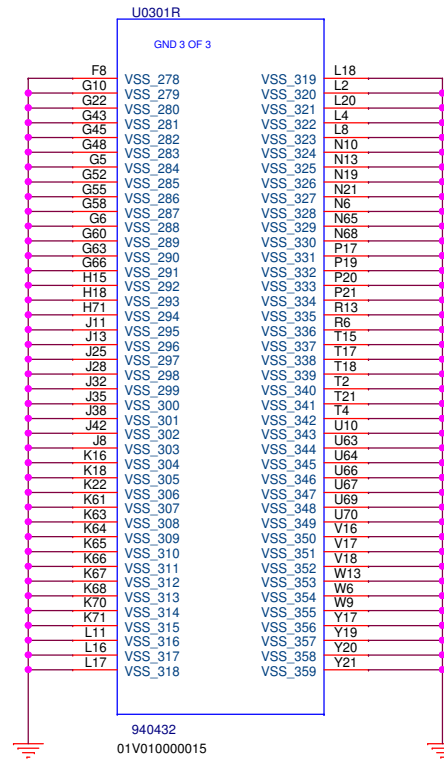
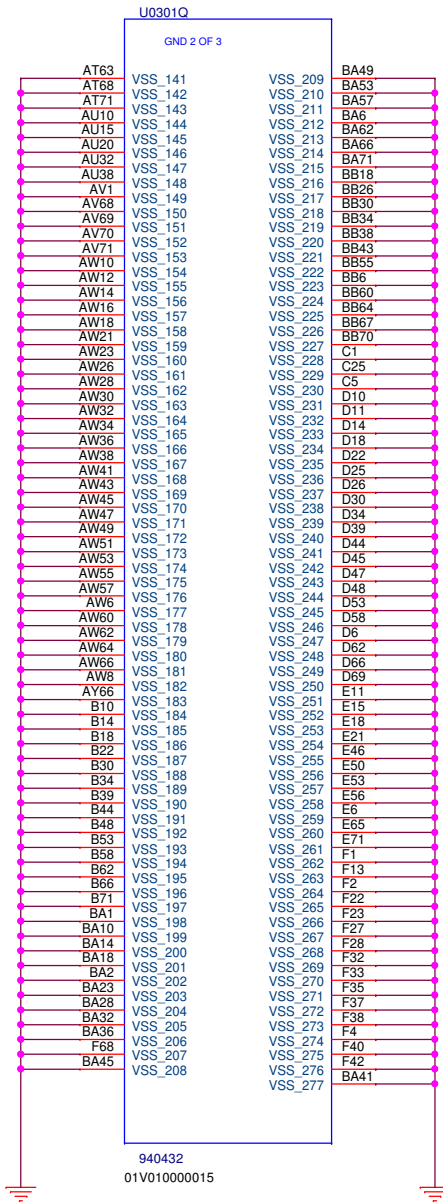
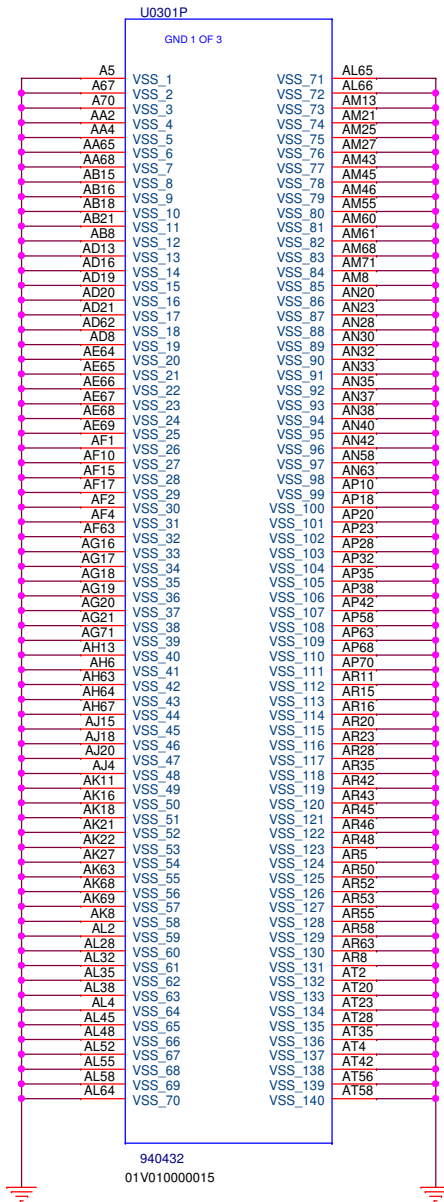










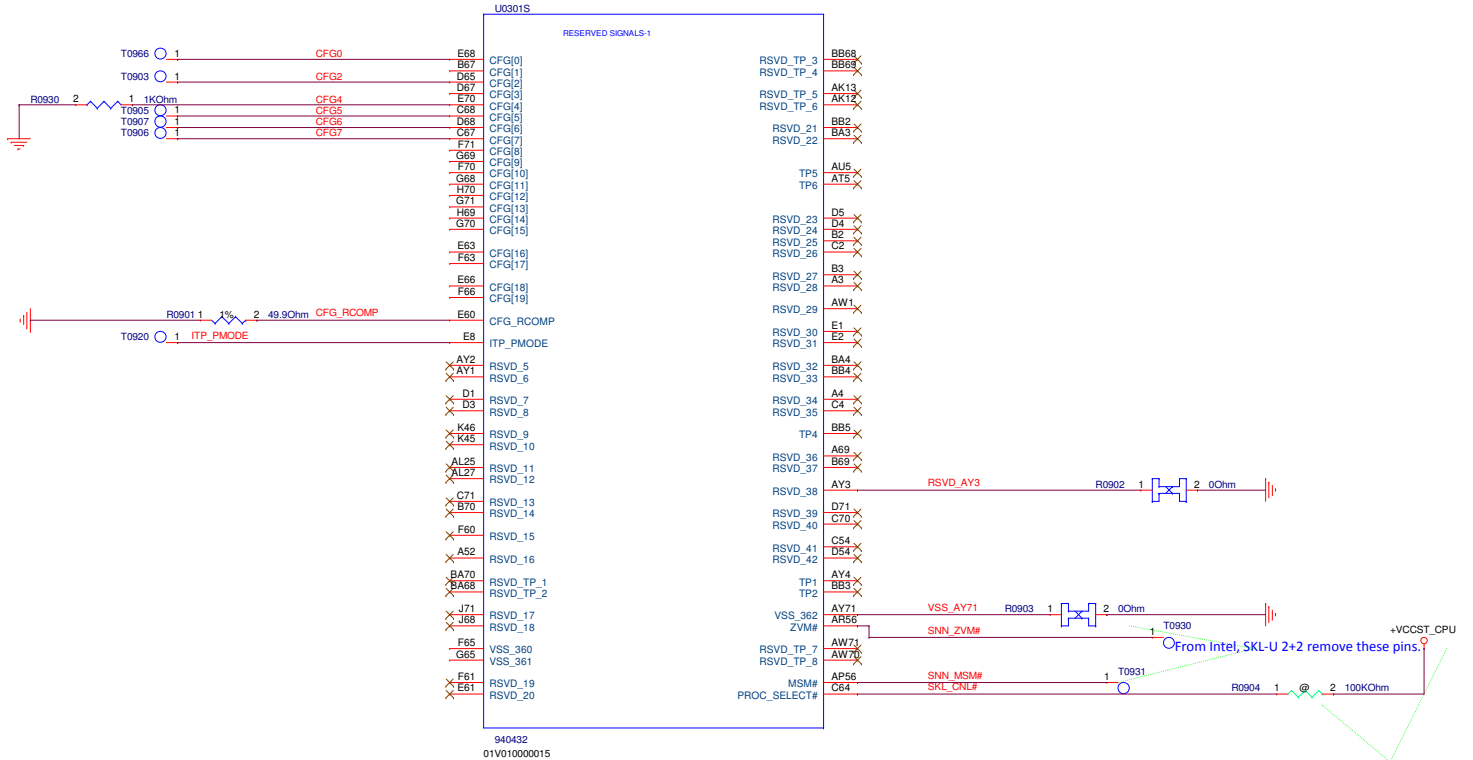




6.4 Reset and Miscellaneous Signals

Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	<p><b>Configuration Signals:</b> The CFG signals have a default value of "1" if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none"><li>• <b>CFG[0]:</b> Stall reset sequence after PCU PLL lock until de-asserted:<ul style="list-style-type: none"><li>— 1 = (Default) Normal Operation; No stall.</li><li>— 0 = Stall.</li></ul></li><li>• <b>CFG[1]:</b> Reserved configuration lane.</li><li>• <b>CFG[2]:</b> PCI Express® Static x16 Lane Numbering Reversal.<ul style="list-style-type: none"><li>— 1 = Normal operation</li><li>— 0 = Lane numbers reversed.</li></ul></li><li>• <b>CFG[3]:</b> Reserved configuration lane.</li><li>• <b>CFG[4]:</b> eDP enable:<ul style="list-style-type: none"><li>— 1 = Disabled.</li><li>— 0 = Enabled.</li></ul></li><li>• <b>CFG[6:5]:</b> PCI Express® Bifurcation<ul style="list-style-type: none"><li>— 00 = 1 x6, 2 x4 PCI Express®</li><li>— 01 = reserved</li><li>— 10 = 2 x8 PCI Express®</li><li>— 11 = 1 x16 PCI Express®</li></ul></li><li>• <b>CFG[7]:</b> PEG Training:<ul style="list-style-type: none"><li>— 1 = (default) PEG Train immediately following RESET# de assertion.</li><li>— 0 = PEG Wait for BIOS for training.</li></ul></li><li>• <b>CFG[19:8]:</b> Reserved configuration lanes.</li></ul>	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.



Intel confirm this pin is pulled high to +VCCST\_CPU for CannonLake

1.3.2 [U] Skylake-U and Cannonlake-U Compatibility Decoupling Requirement

Two reserve pins (U11 and U12) for 1.8V were added to Skylake-U PCH to support Cannonlake-U PCH compatibility. For Skylake-U, the following changes will be made to Table 52-8 in the Skylake U/Y Platform Design Guide (1BP#543016).

Table 52-8 - Decoupling and Power Connection Requirement for Skylake-U PCH

Voltage Supply	Area	PCB Pin sharing power rail	Value	Size	Quantity	Placement Type (1 memory / 10 Jdgs)	Place constraint(s) near ball(s)
V1.8A	VCCPGPF	AP16	-	-	-	-	-
	VuATS	AA1	1 uF	0402	1	E (<10 mm)	AA1
	VCC_1P8	U13, U12	1 uF	0402	1	E (<10 mm)	U11, U12 (Note 1 & 5)

D

1

C

1

B

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A

1

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PEGATRON PROPRIETARY AND CONFIDENTIAL

PEGATRON PROPRIETARY AND CONFIDENTIAL

**Engineer:**

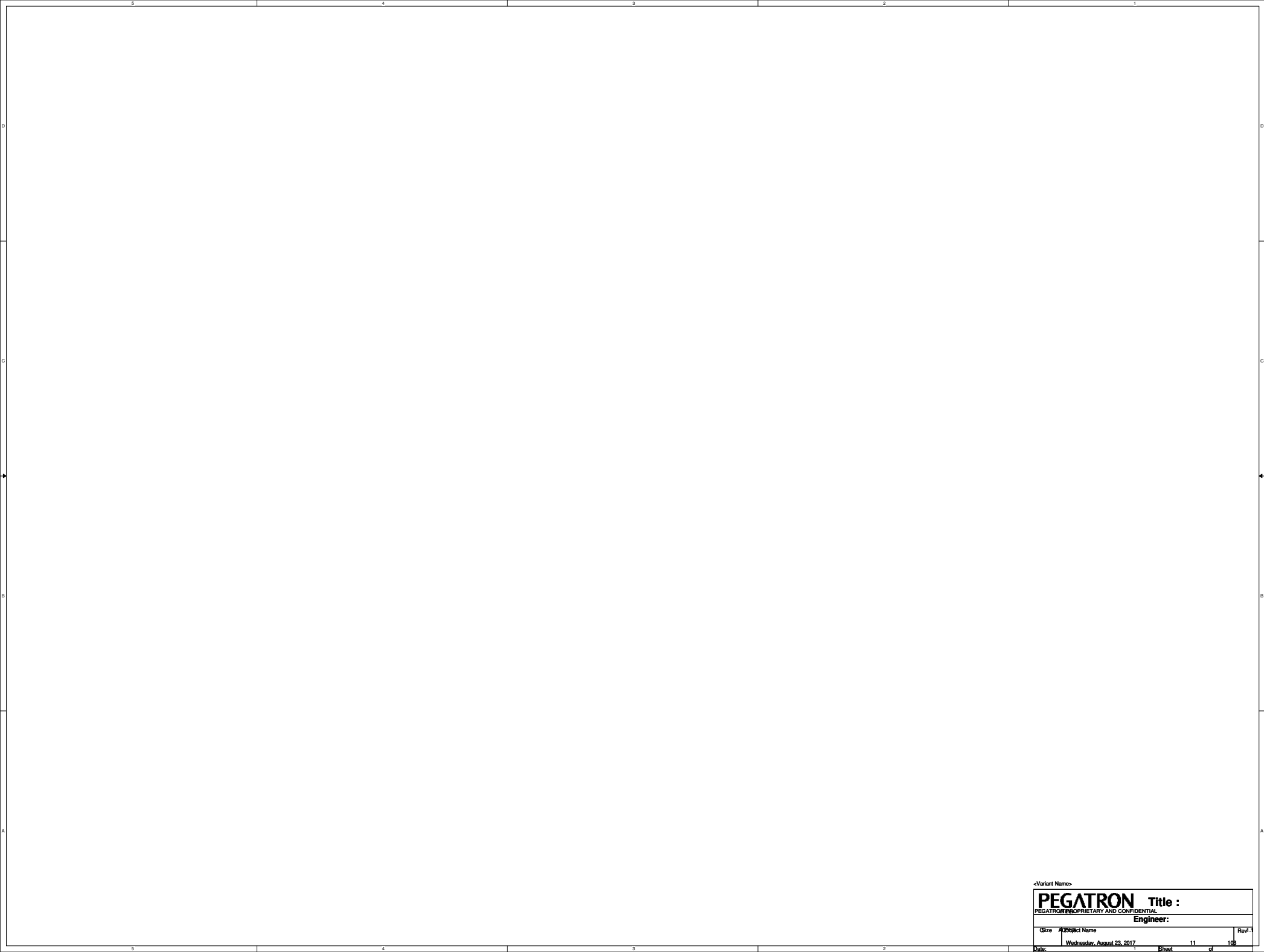
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Wednesday, August 23, 2017

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Date: Wednesday, August 23, 2017 Sheet 12 of 108

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Date: Wednesday, August 23, 2017 Sheet 12 of 108

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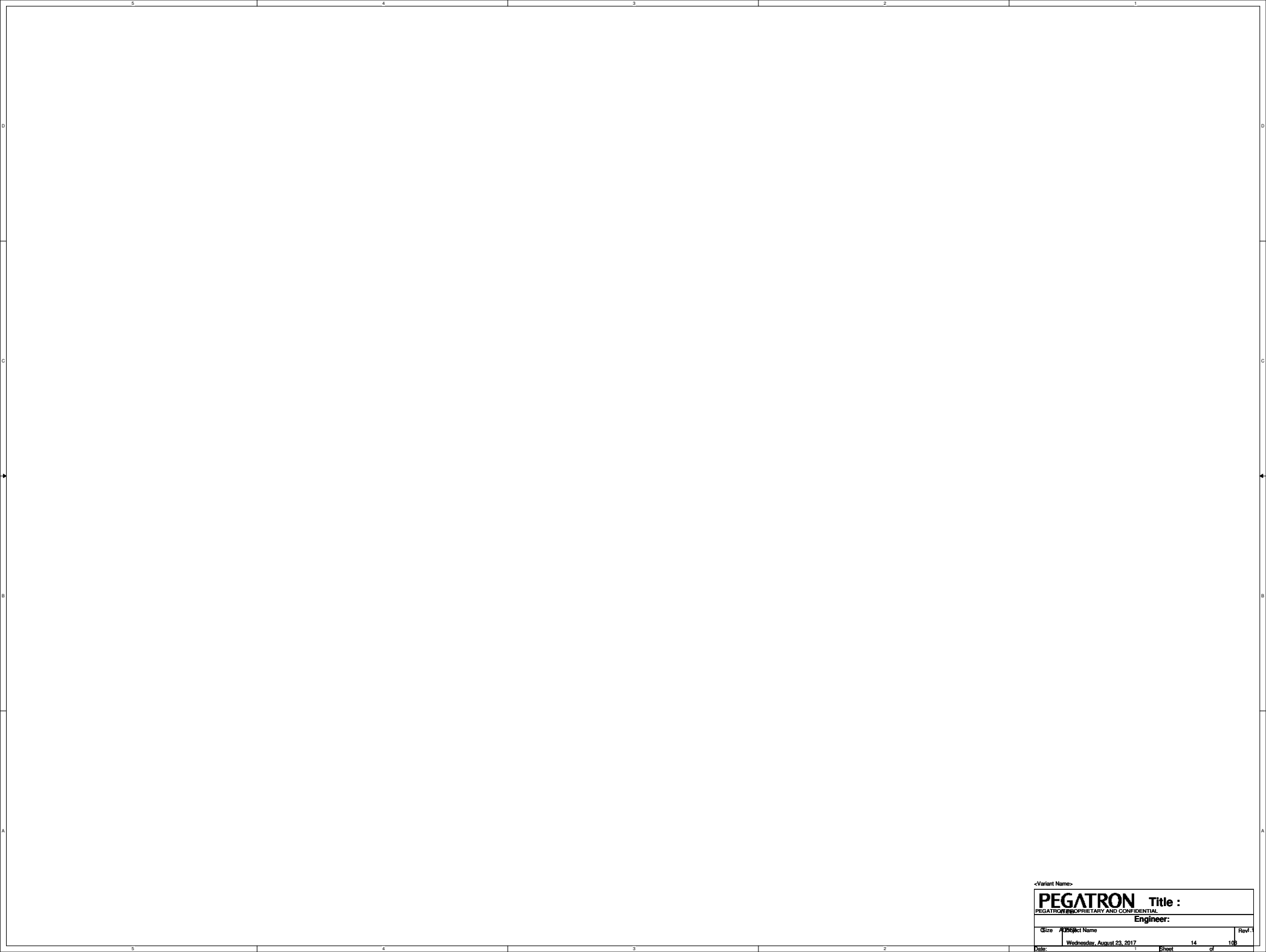
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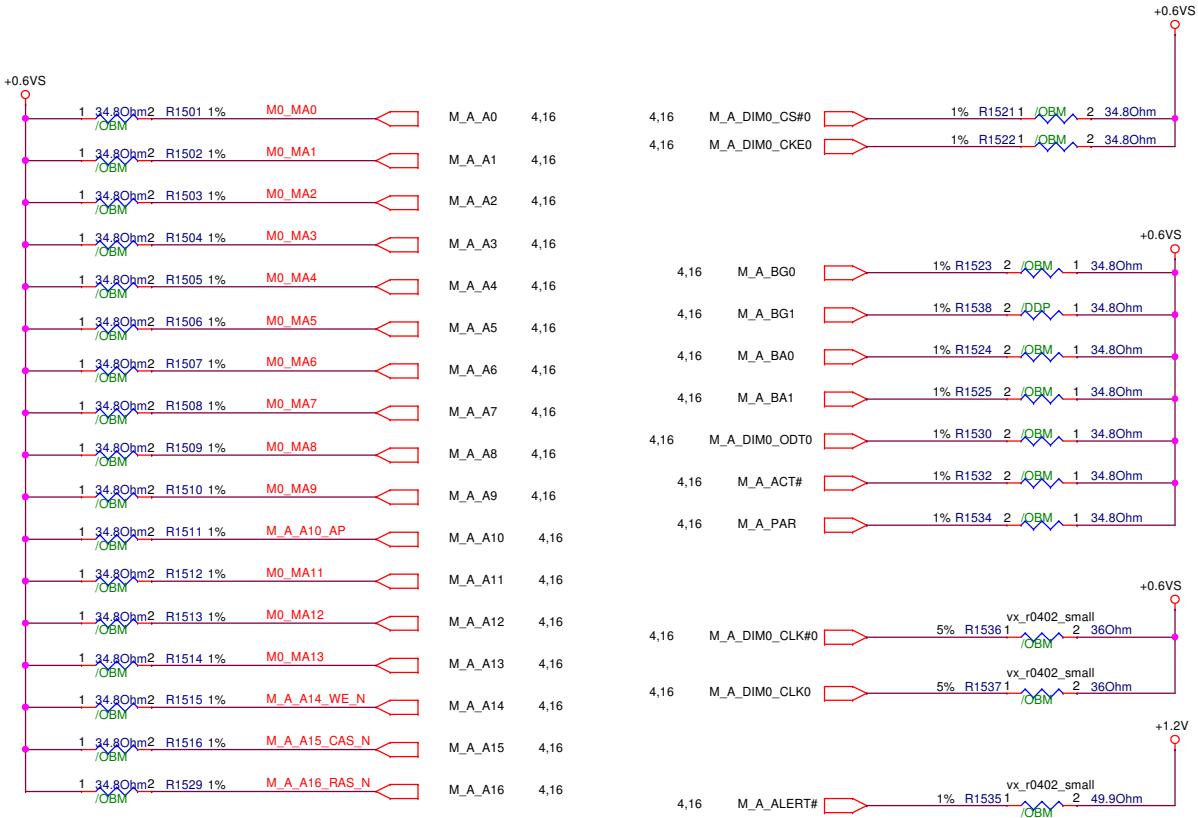




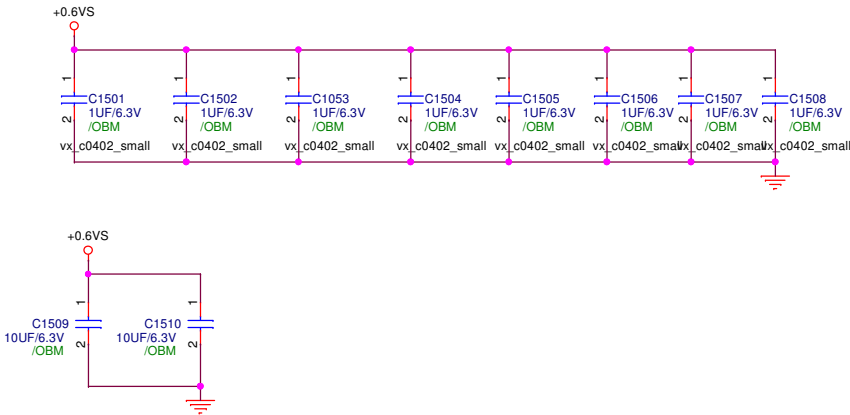
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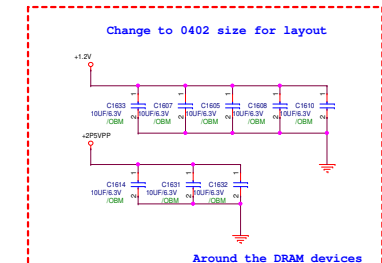
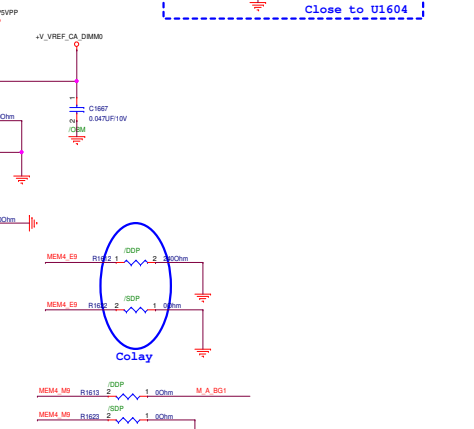
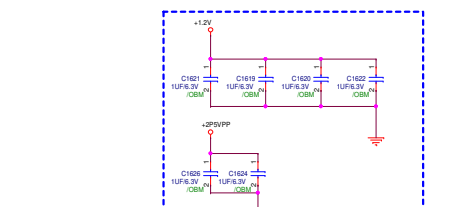
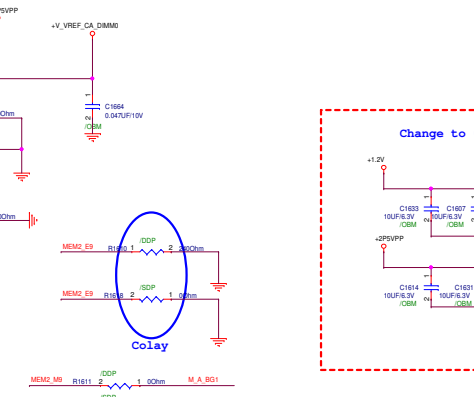
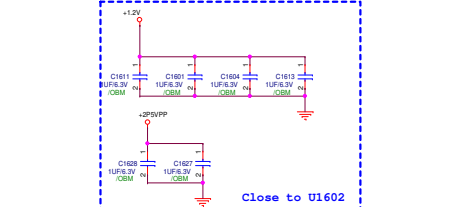
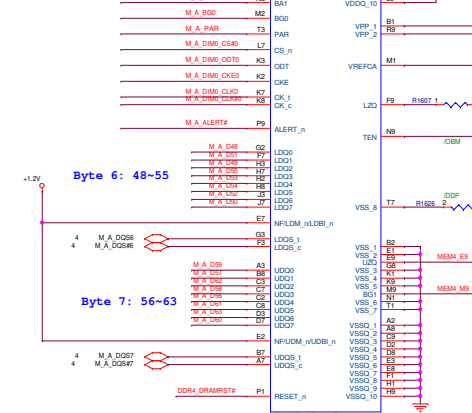
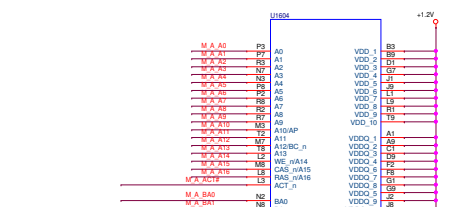
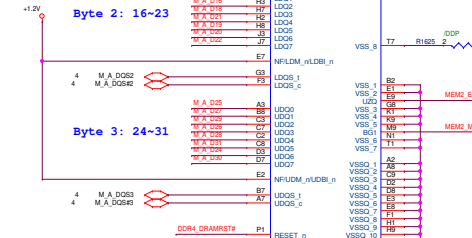
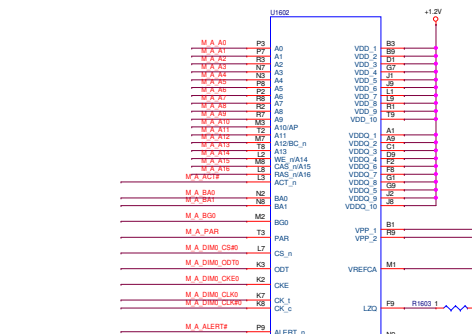
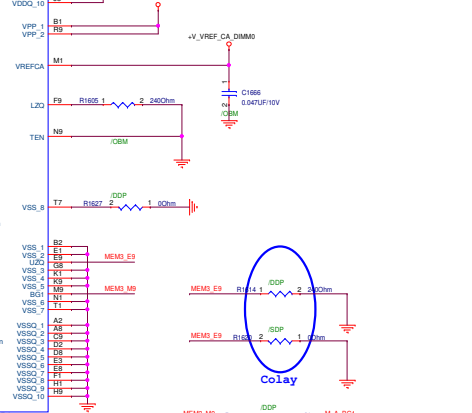
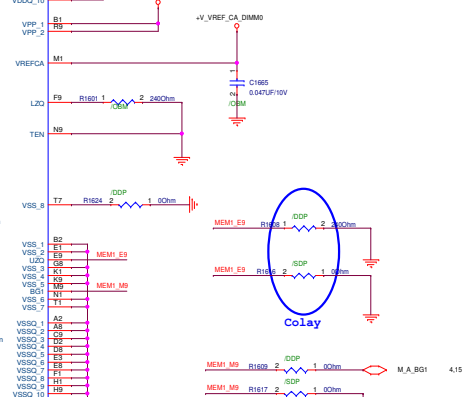
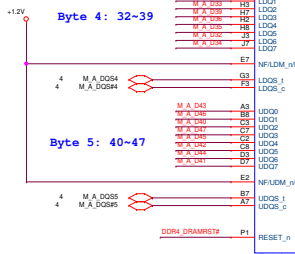
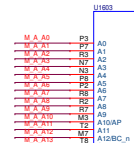
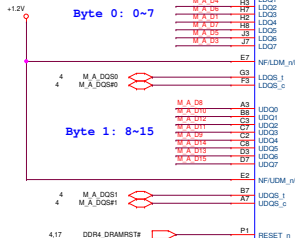
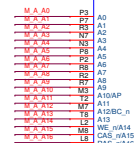
DDR4(0)\_Termination

+0.6VS +0.6VS 17,57,83  
+1.2V +1.2V 4,7,16,17,18,57,83



Average placed close to +VDDQ\_VTT power plane



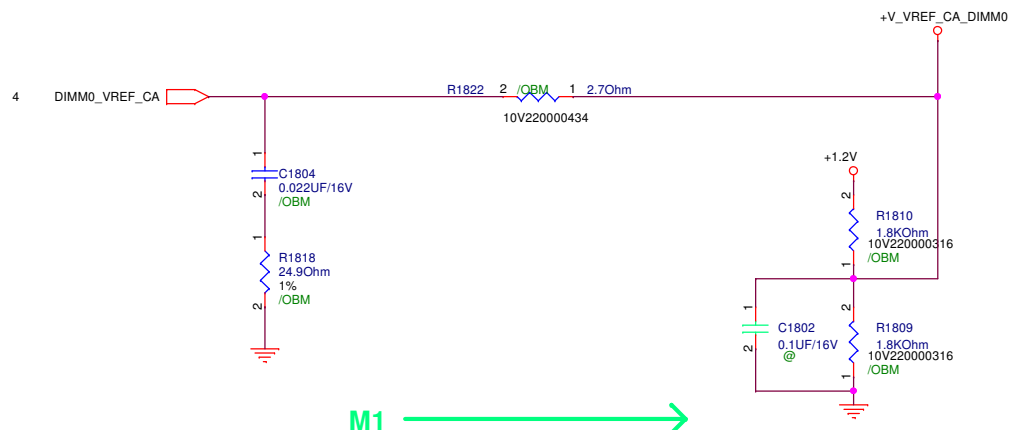




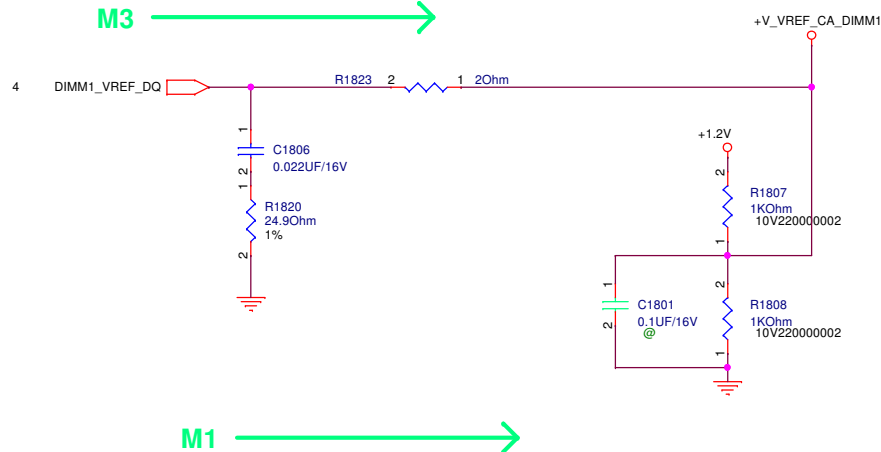


M3: CPU driven VREF path is stuffed be default.  
M1: VREF\_DQ driven by a Voltage Divider Network during Processor power-off

M3 →



M3 →



+1.2V

+V\_VREF\_CA\_DIMM0

+V\_VREF\_CA\_DIMM1

+1.2V

+V\_VREF\_CA\_DIMM0

+V\_VREF\_CA\_DIMM1

4,7,15,16,17,57,83

16

17

Figure 4-46. SKL U DDR4/-RS x16 Devices Memory Down V<sub>REF-CA</sub> Overview

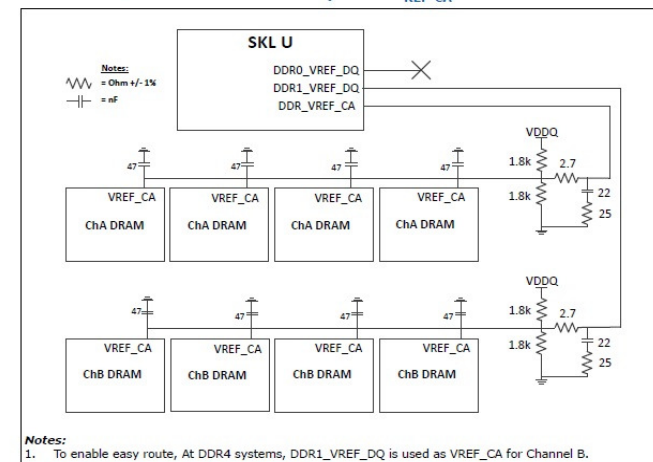
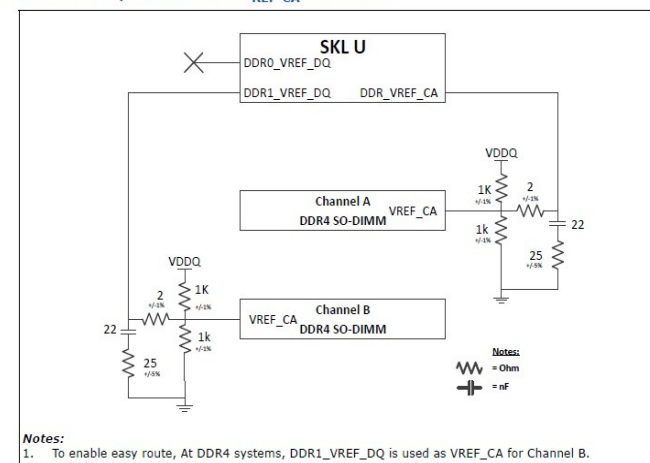
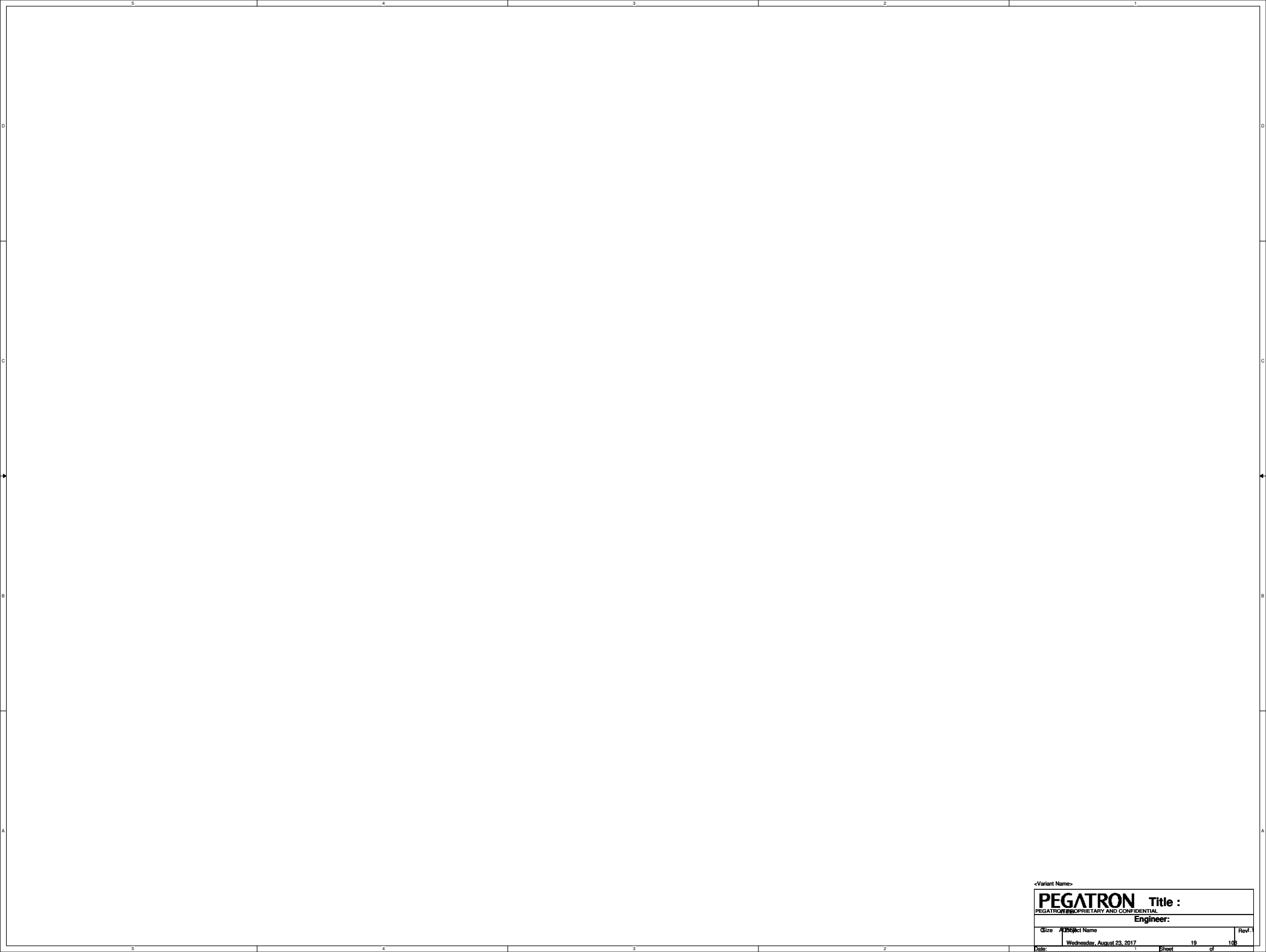


Figure 4-45. SKL U DDR4/-RS SODIMM V<sub>REF-CA</sub> Overview

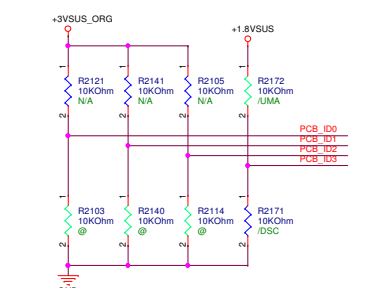


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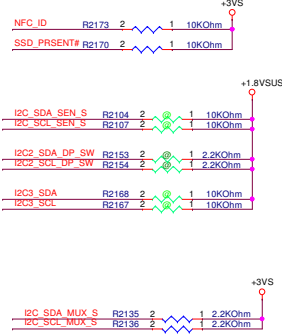
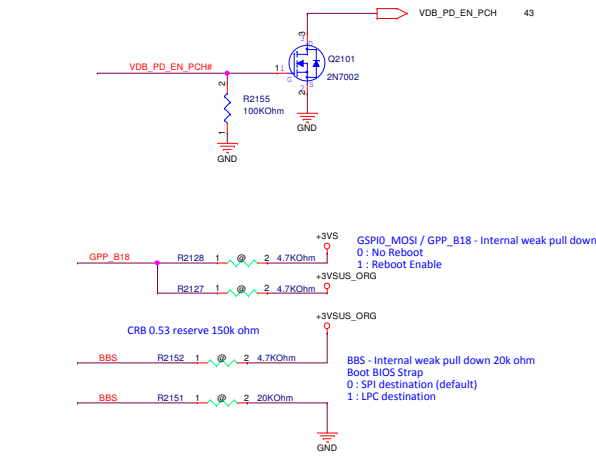
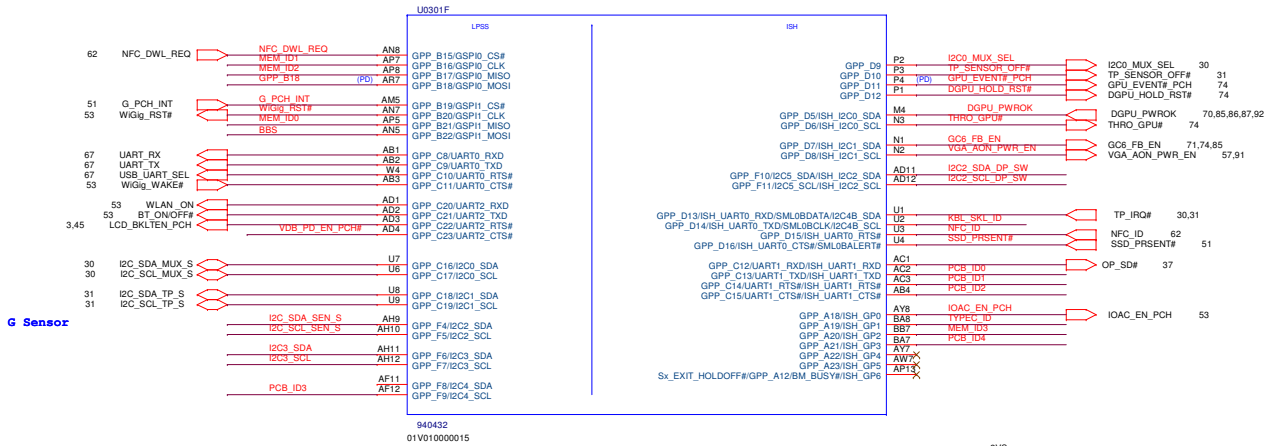
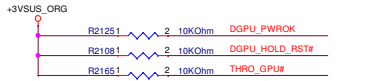
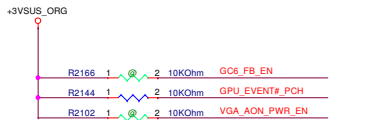
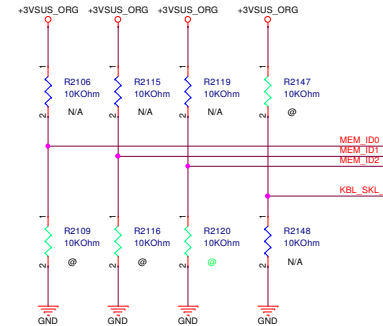


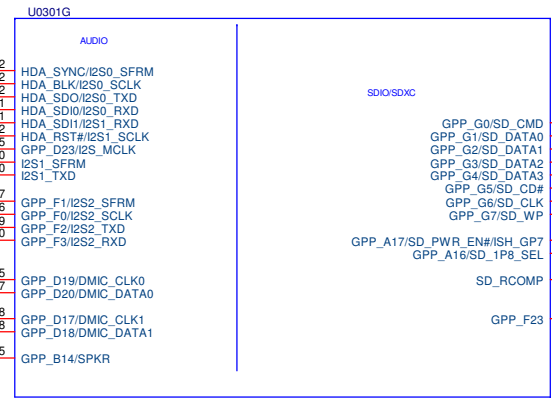
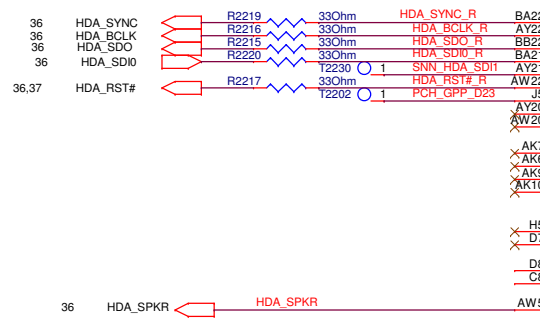
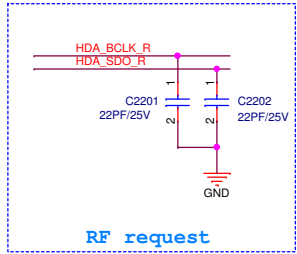
ID2	ID1	ID0	PCB Rev.
0	0	0	R1.0
0	0	1	R1.1
0	1	0	R2.0
0	1	1	R2.1
1	0	0	TBD
1	0	1	TBD
1	1	0	TBD
1	1	1	P2

MEM_ID0	MEM_ID1	MEM_ID2	Memory Setting
0	0	0	SAMSUNG/K4A1G165WD-BCPB-4Gb-256Mb*16-0315-01C70PB
1	0	0	HYNIX/H5ANAG6NAMR-UHC 0315-02640PB HYNIX DDP 8G
0	1	0	SAMSUNG/K4A8G165WB-BCPB 8Gb 512Mb*16-0315-01HF0PB
1	1	0	DR4 2400 1Gb*16 1.2V FBGA96 MICRON/MT40A1G16WBU-083E:B 0315-01YC0PB NEW Micron DDP for 8L
0	0	1	SAMSUNG/K4A8G165WB-BCRC 2400 512Mb*16 0315-01C80PB
1	0	1	SK HYNIX/H5AN8G6NAFR-UHC 2400 512Mb*16 0315-01W60PB
0	1	1	MICRON/MT40A512M16JY-083E:B 2400 512Mb*16 0315-01W90PB
1	1	1	DR4 2400 1Gb*16 1.2V FBGA96 MICRON/MT40A1G16WBU-083E:B 0315-01YC0PB old Micron DDP for 6L

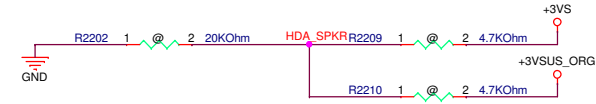


KBL_SKL_ID	SSD_PRESNT#	NFC_ID	PCB_ID3	TYPEC_ID
1:SKL	1: No SSD	1: No NFC	1: UMA	1: RTS5440
0: KBL	0: SSD	0: NFC	0: DSC	0: ANX7428





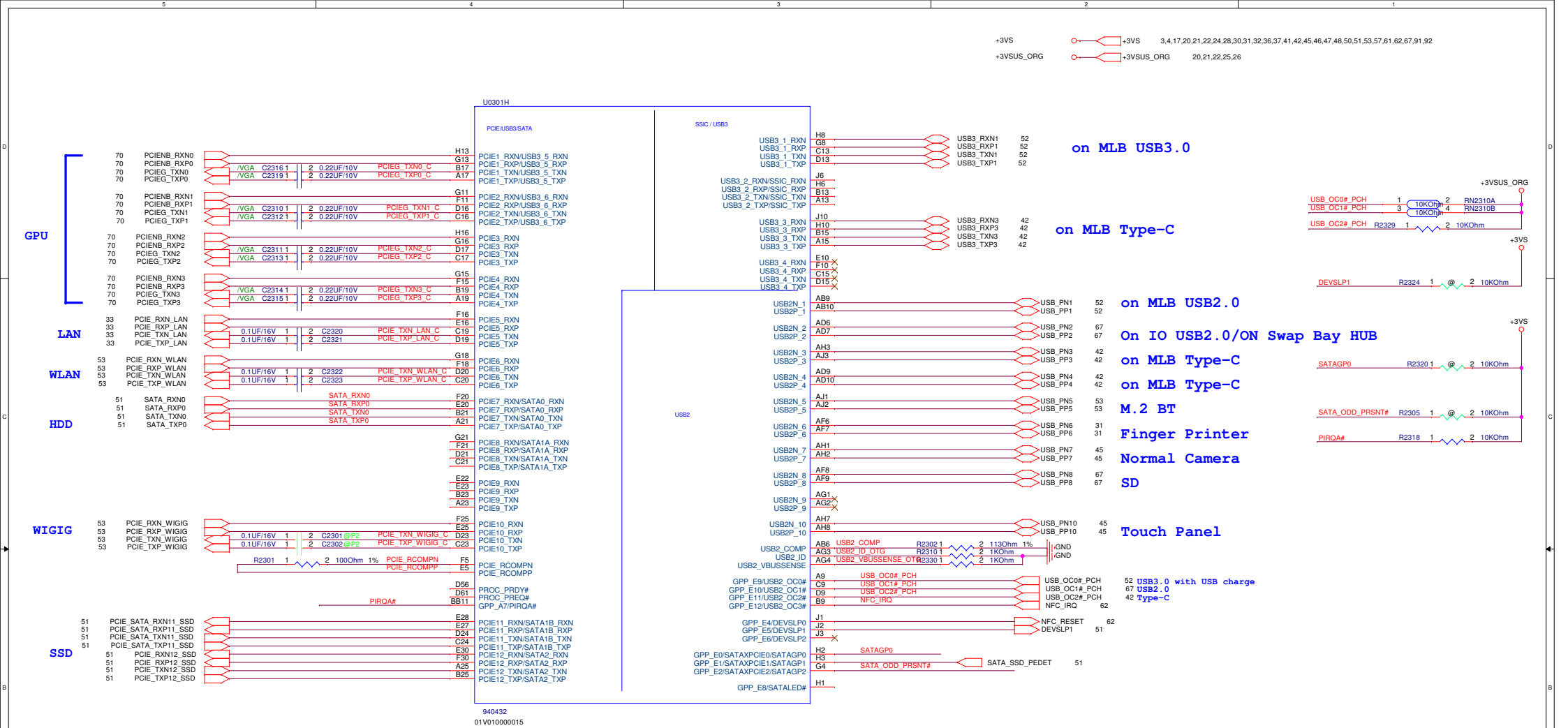
940432  
01V010000015



HDA\_SDO - Internal weak pull down  
FLASH\_DESCRIPTOR SECURITY OVERRIDE  
0 : Enable  
1 : Disable

+3VS  
+3VSUS\_ORG

SPKR - Internal weak pull down  
0 : Disable TOP Swap mode (default)  
1 : Enable Top Swap Enable  
  
Default is GPO, to reserve pull high to +3VSUS\_ORG



### 3.4.1 SKL PCH U Flexible I/O

Figure 3-1. HSIO Muxing on SKL PCH U

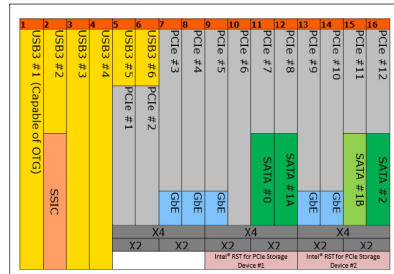


Table 1-2. PCH-LP SKUs (Sheet 2 of 2)

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Total Intel® RST capable PCIe and SATA Express <sup>4</sup> Storage Devices	0	2	2

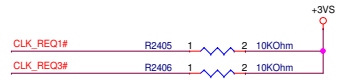
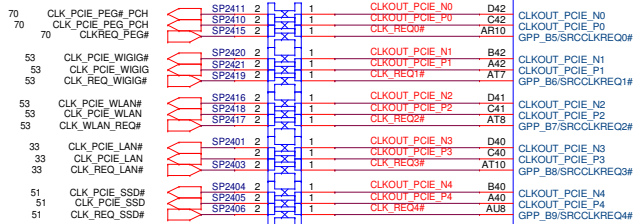
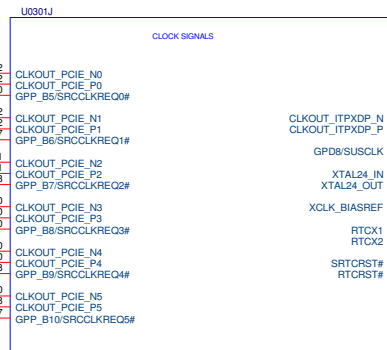
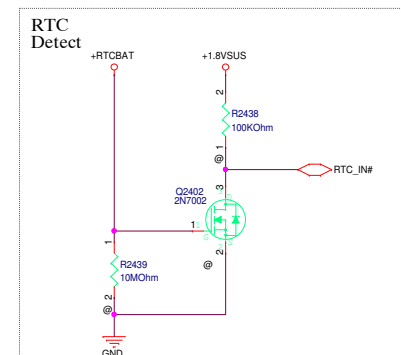
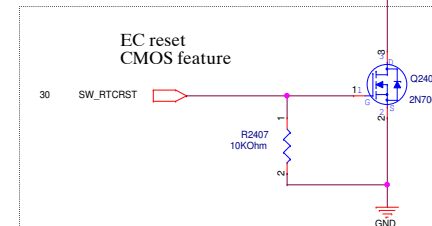
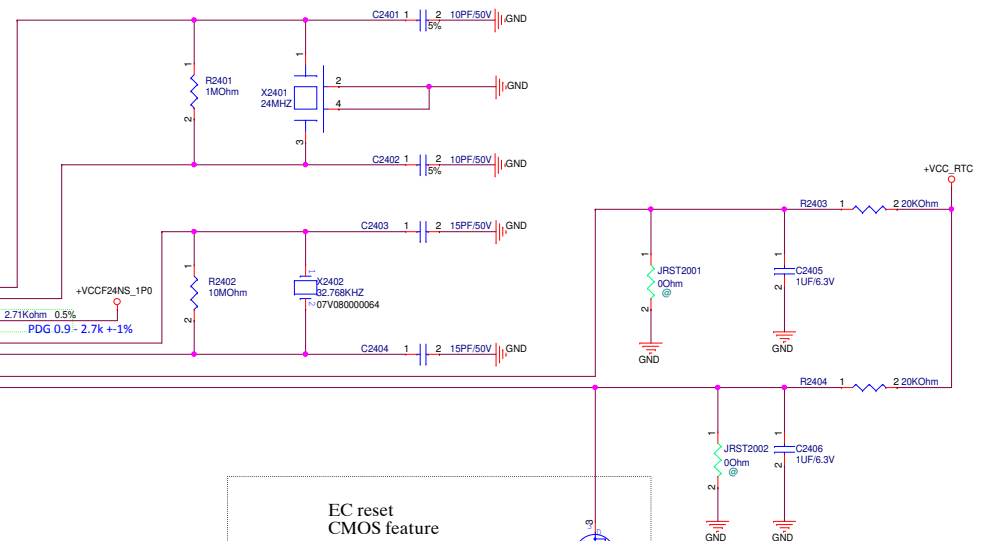
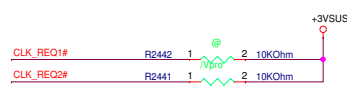
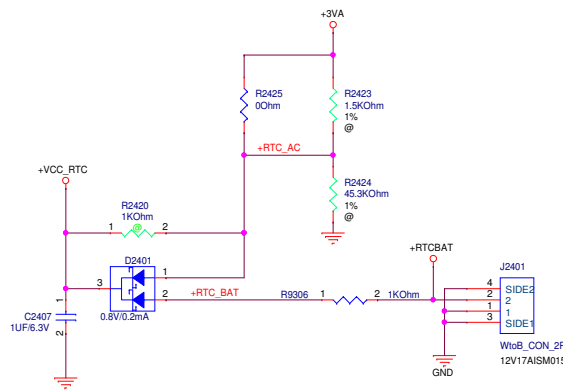
**Notes:**

1. USB 2.0 port numbers: 1-8
2. USB 2.0 port numbers: 1-10
3. USB 2.0 port numbers: 1-6
4. SATA Express Capable Ports (x2)

Table 1-3. PCH-LP HSIO Detail

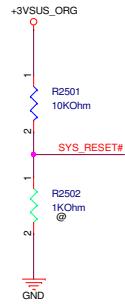
SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0 OTG	USB 3.0 SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/LAN	PCIe/LAN	PCIe/LAN	PCIe	SATA	SATA	PCIe/LAN	PCIe/LAN	N/A	N/A
Premium-U	USB 3.0 OTG	USB 3.0 SSIC	USB 3.0	USB 3.0	PCIe/LAN	PCIe/LAN	PCIe/LAN	PCIe/LAN	PCIe/LAN	PCIe	SATA	SATA	PCIe/LAN	PCIe/LAN	SATA	SATA
Premium-Y	USB 3.0 OTG	USB 3.0 SSIC	USB 3.0	USB 3.0	PCIe/LAN	PCIe/LAN	PCIe/LAN	PCIe/LAN	PCIe/LAN	PCIe	SATA	SATA	PCIe/LAN	PCIe/LAN	N/A	N/A

<Variant Name>

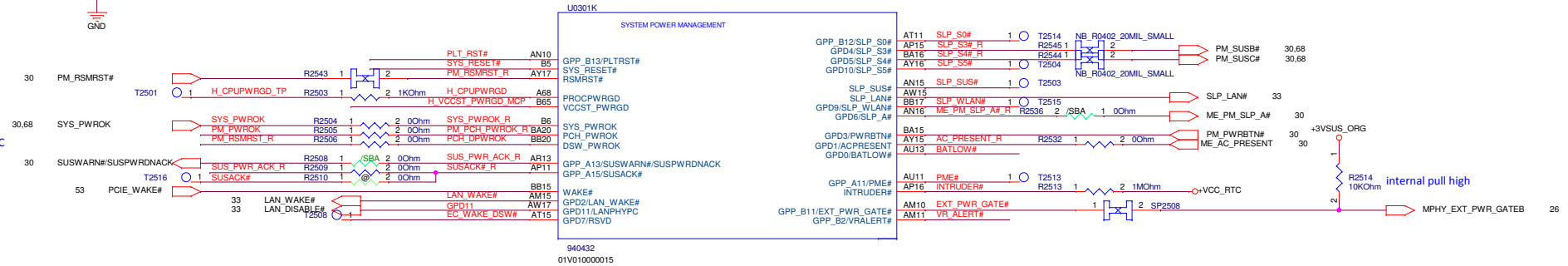
[illegible]

<b>PEGATRON</b> <b>THIN</b> PEGATRON PROPRIETARY AND CONFIDENTIAL		CLK, RTC, HDA, SDIO	
<b>Engineer:</b> <i>Bill Yang</i>			
BG1/HW3 Size Custom	Project Name <b>AQ5EB</b>		Rev 1.0
Date: <u>Wednesday, August 23, 2017</u>	Sheet <u>24</u> of <u>108</u>		

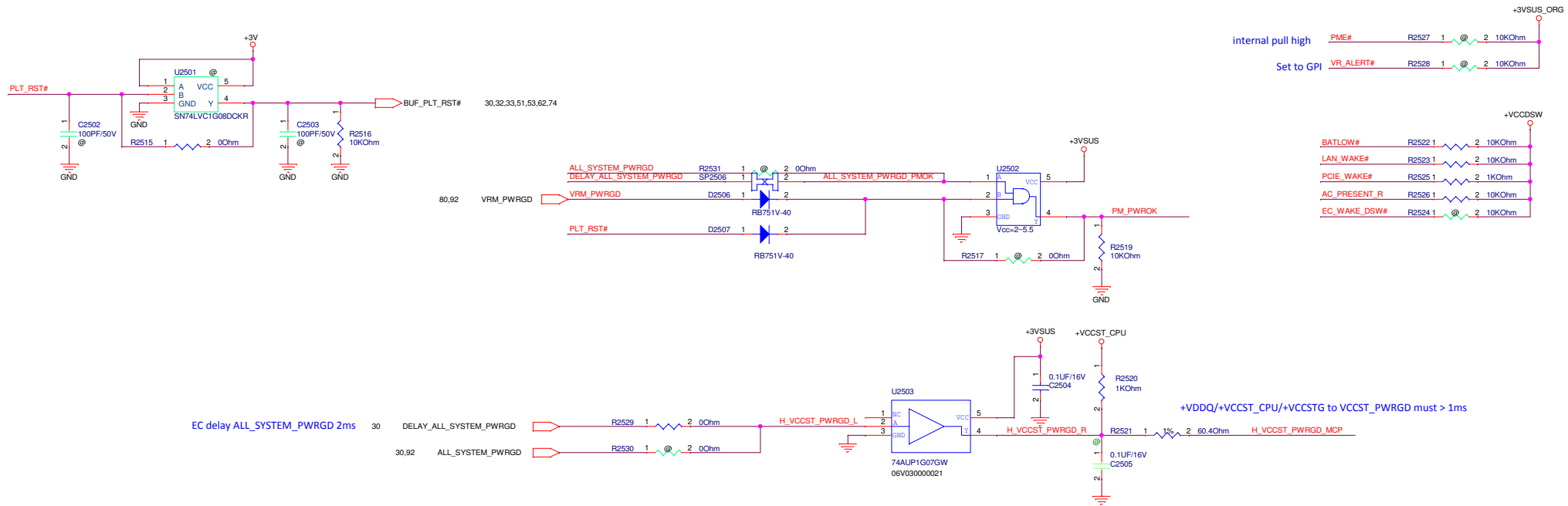




+3VSUS		+3VSUS	4,24,26,28,30,31,33,42,51,53,62,67,68,81,92
+VCCDSW		+VCCDSW	26,30
+3VSUS_ORG		+3VSUS_ORG	20,21,22,23,26
+3V		+3V	31,41,44,57,67,82,91
+VCC_RTC		+VCC_RTC	24,26,36,60
+VCCST_CPU		+VCCST_CPU	3,5,7,9

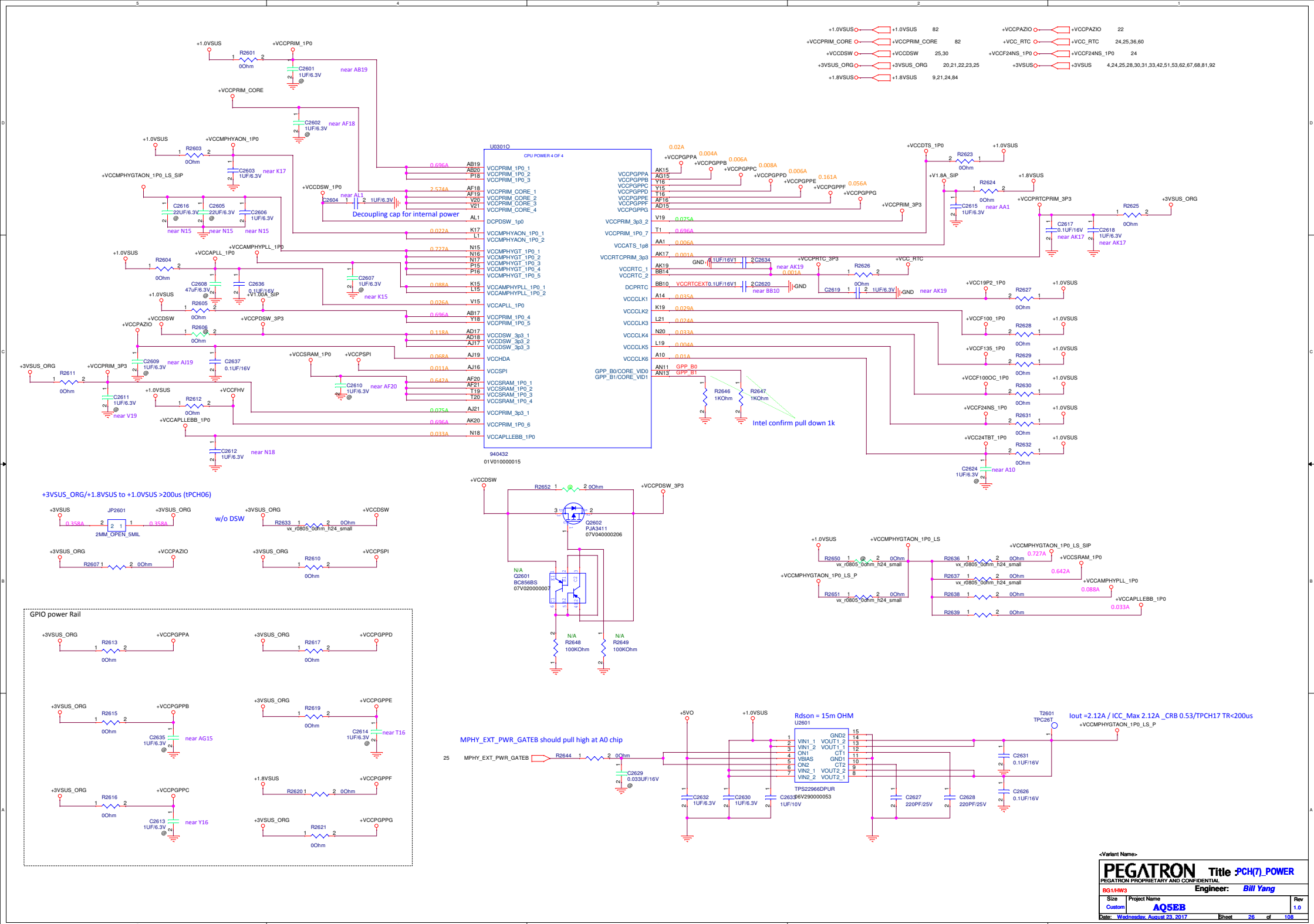


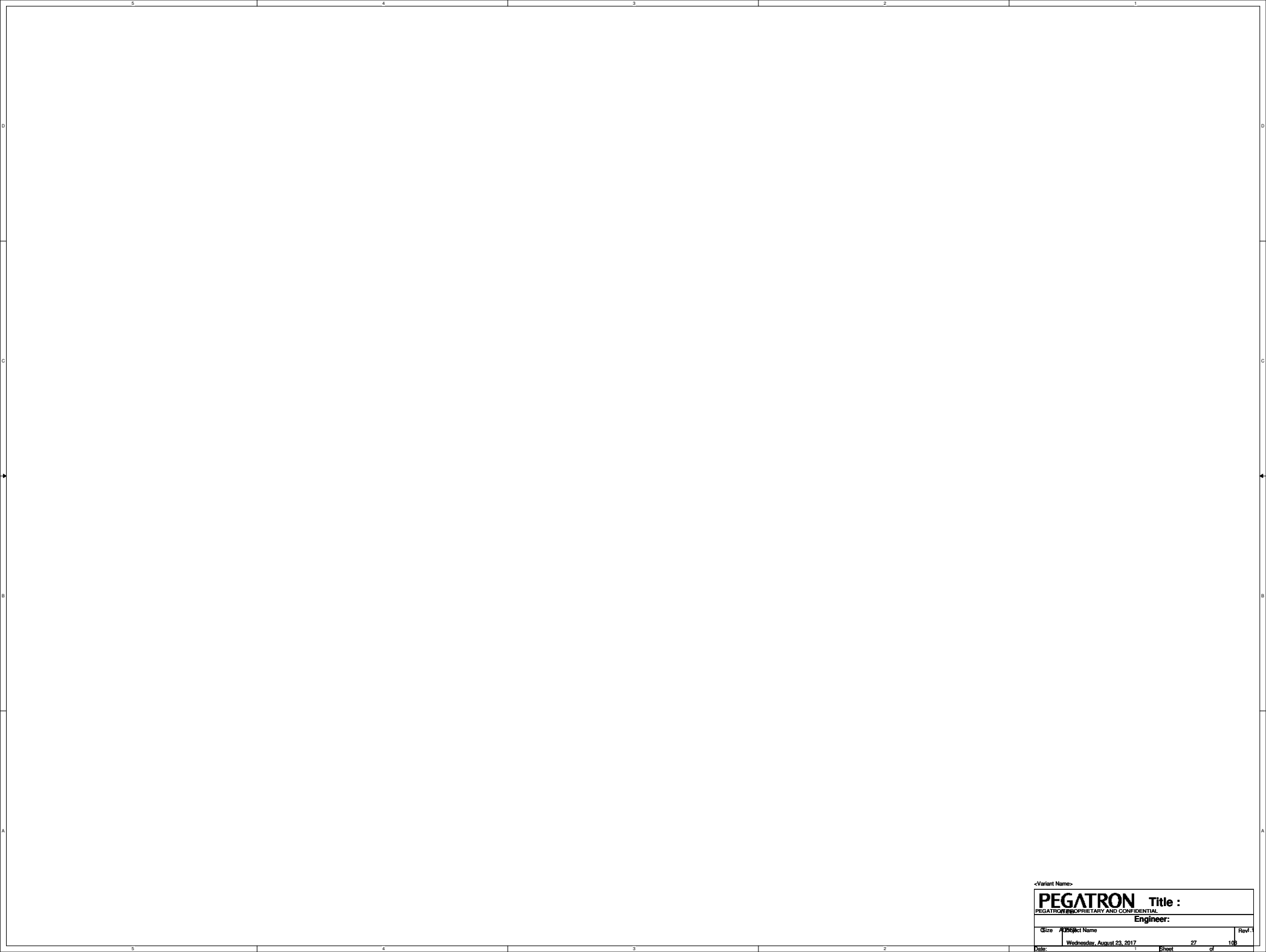
ALL\_SYS\_PWRGD delay 99 ms from EC



EC delay ALL\_SYSTEM\_PWRGD 2ms

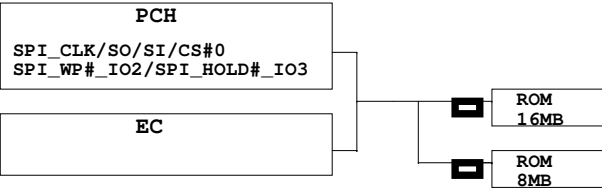
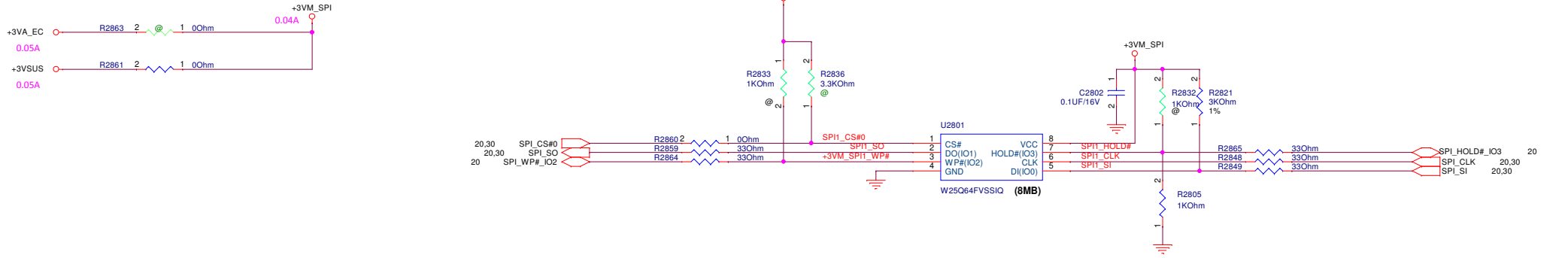
+VDDQ/+VCCST\_CPU/+VCCSTG to VCCST\_PWRGD must > 1ms



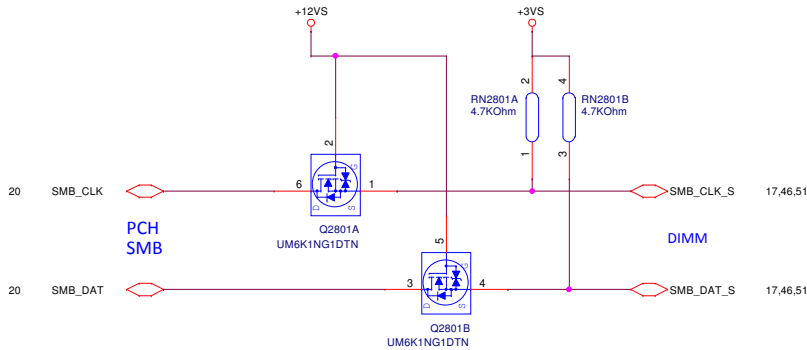


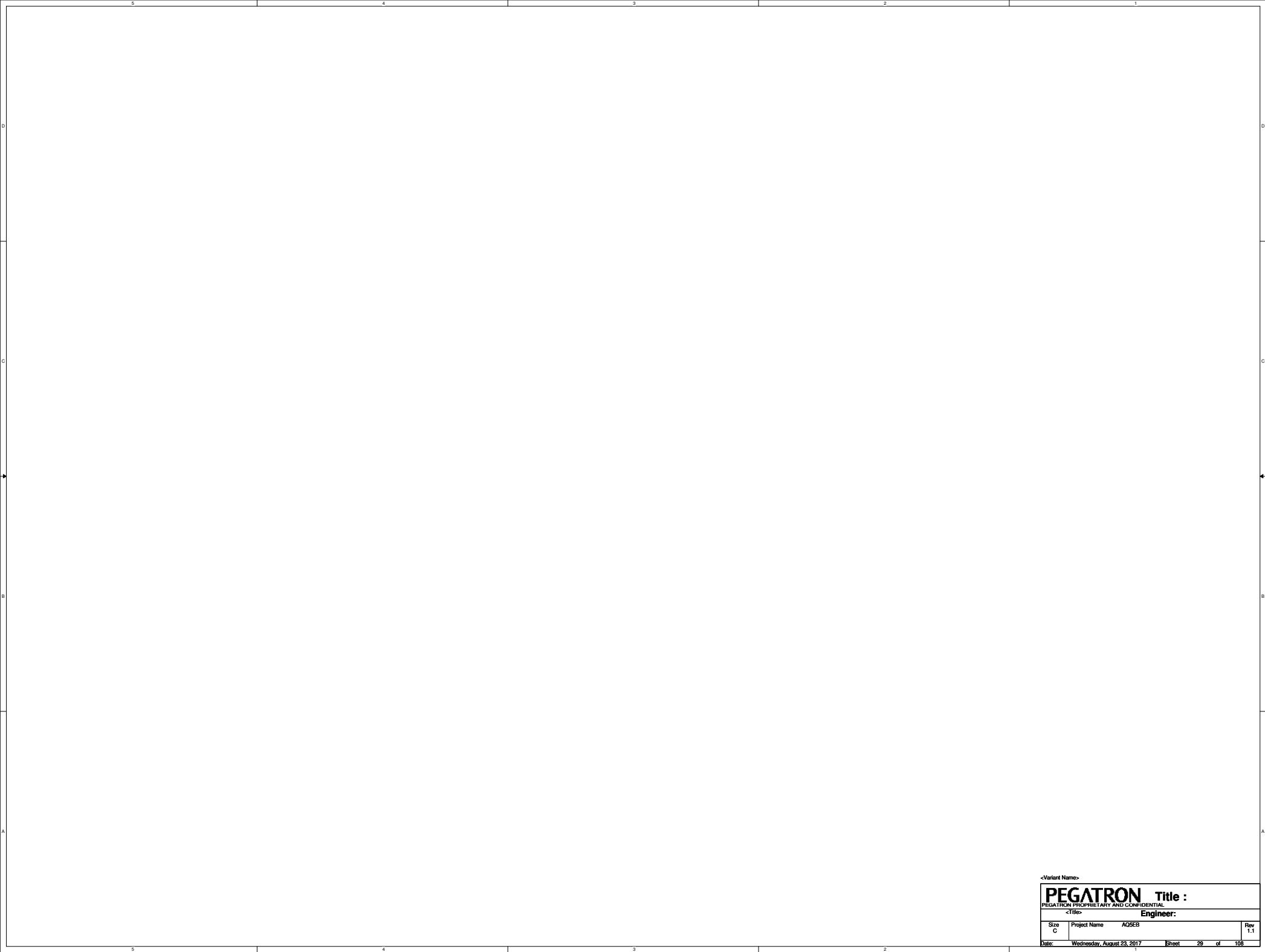
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<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		<b>Engineer:</b>	
Size	Subject Name	Date	Rev.
	Wednesday, August 23, 2017	Sheet 27 of 108	

PCH SPI ROM



PCH SMBus

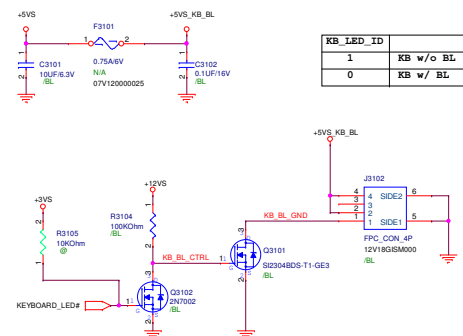




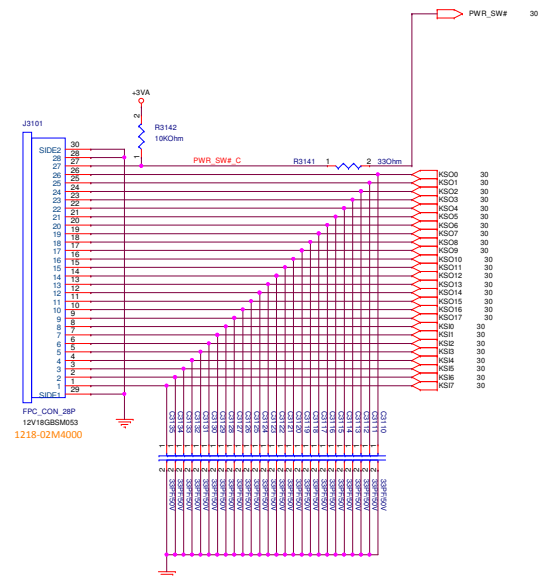
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<b>PEGATRON</b> Title :		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<Title> Engineer:		
Size C	Project Name AQ5EB	Rev 1.1
Date:	Wednesday, August 23, 2017	Sheet 29 of 108



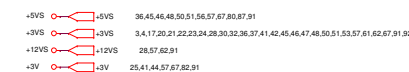
## Keyboard LED



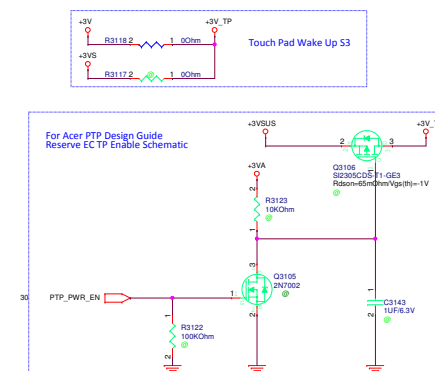
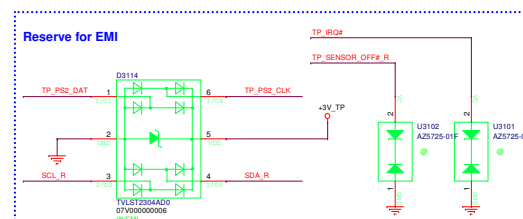
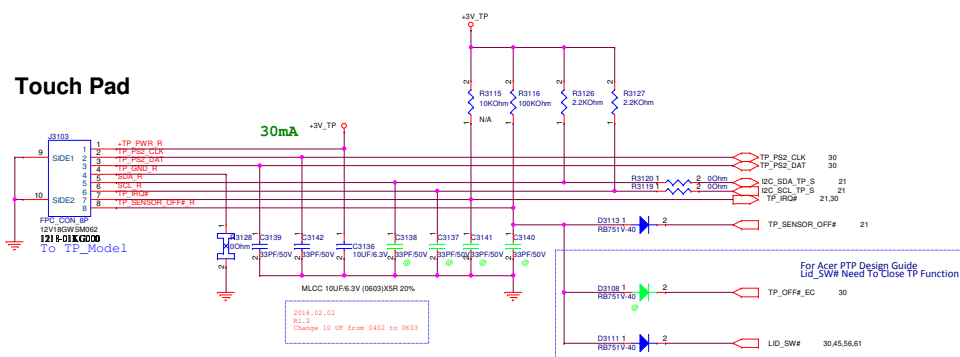
## Keyboard



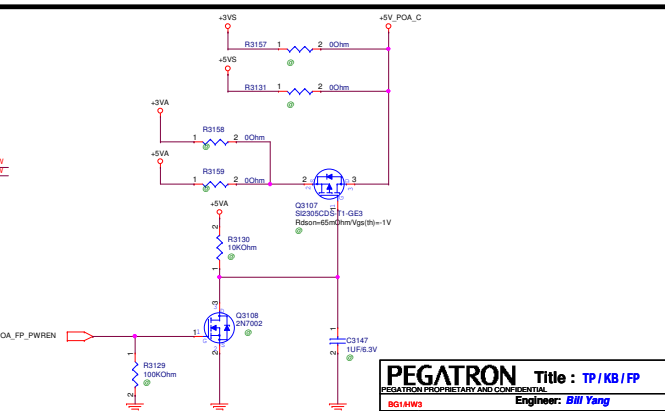
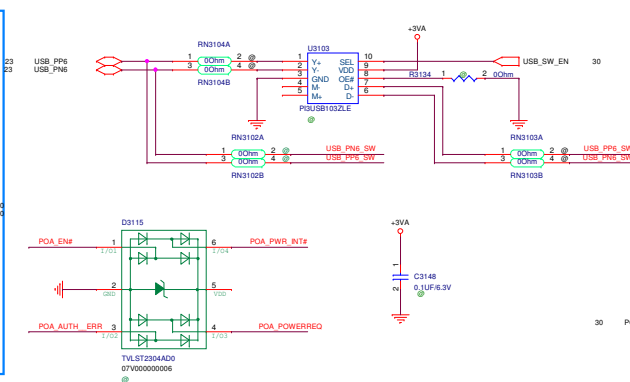
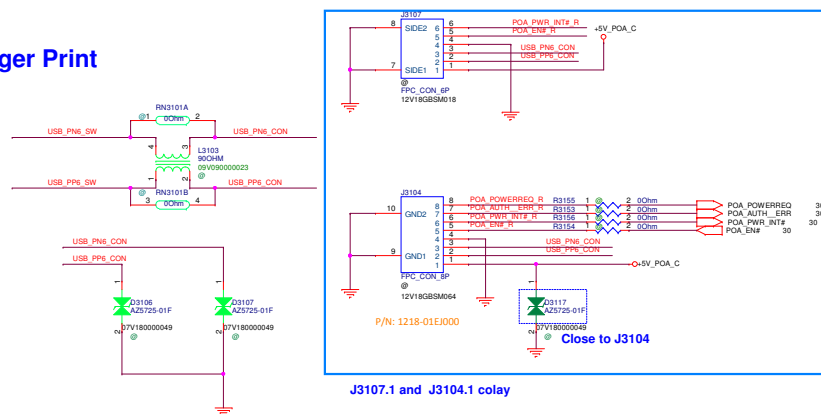
for Top/Bot side 各一 (開機測點) 6/2



## Touch Pad

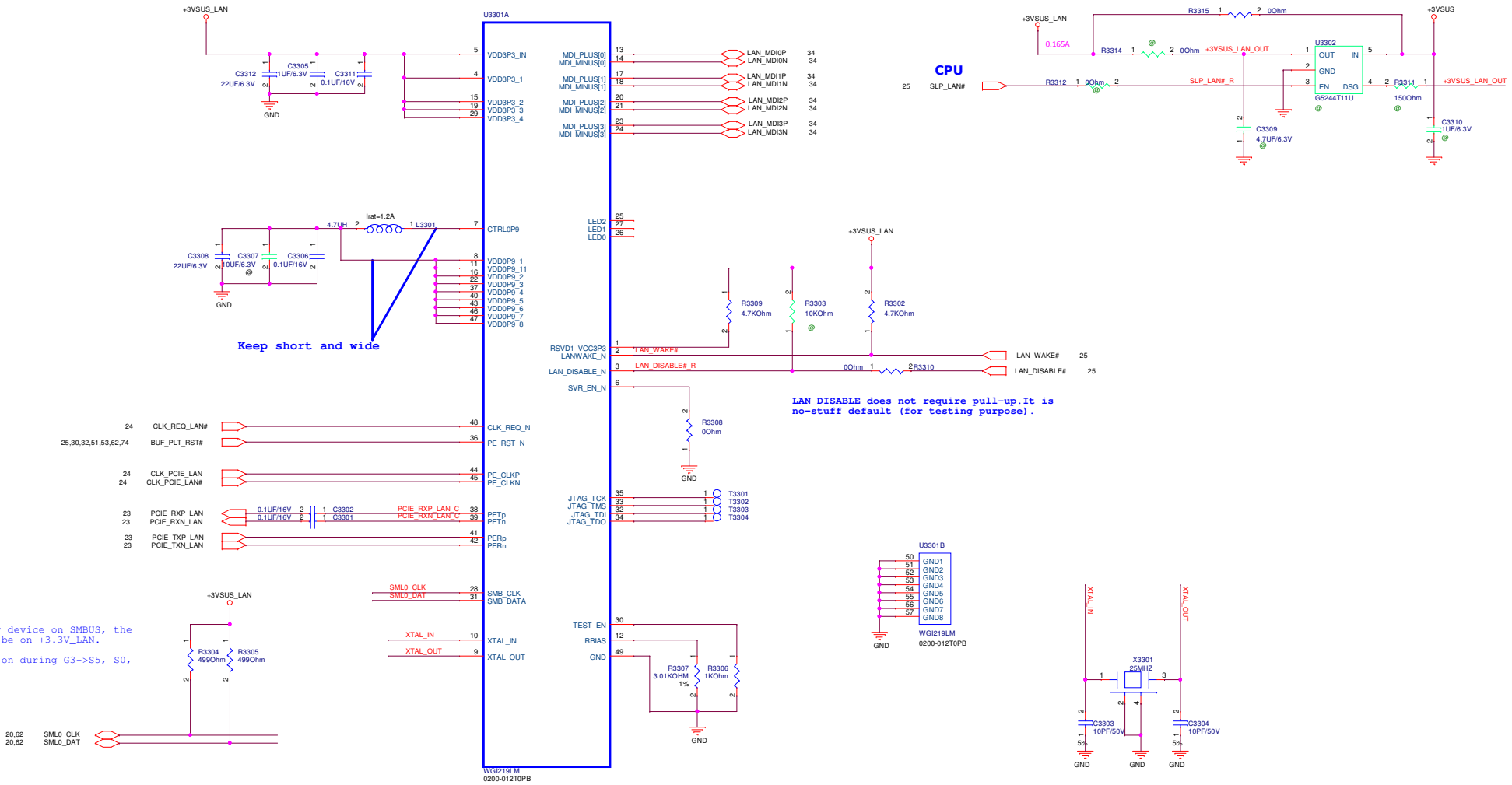


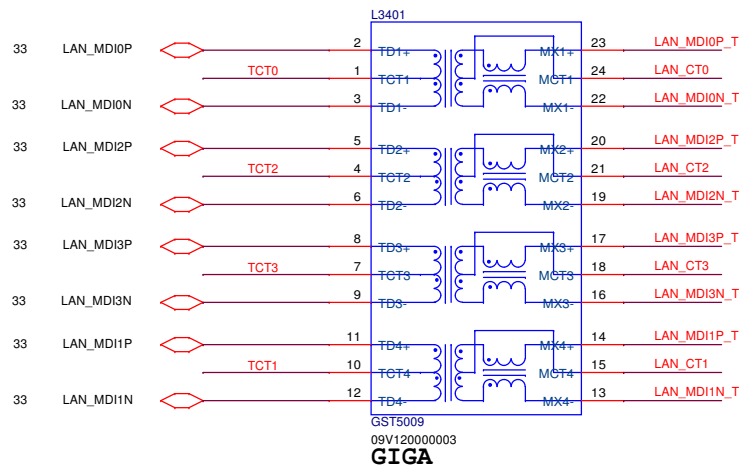
## Finger Print



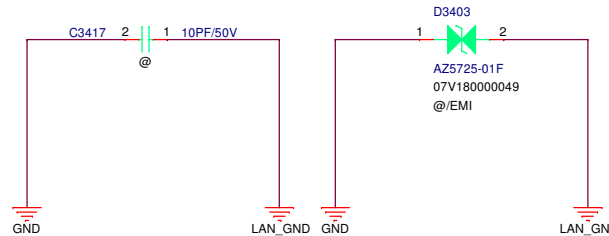
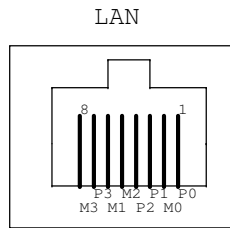
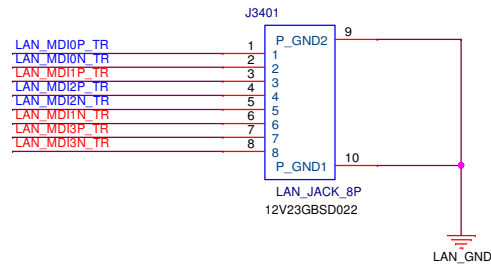
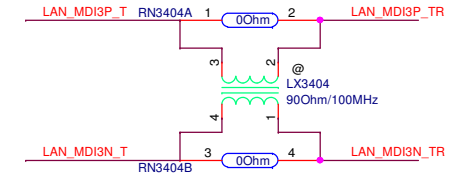
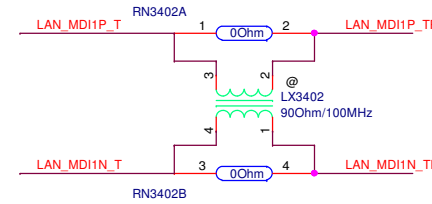
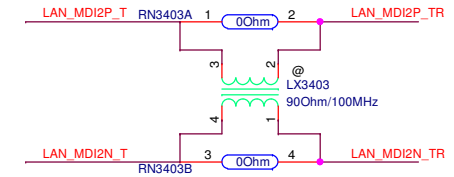
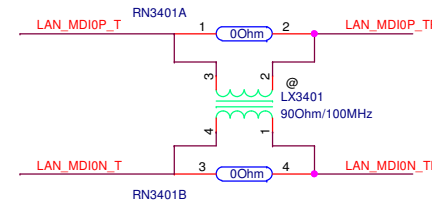
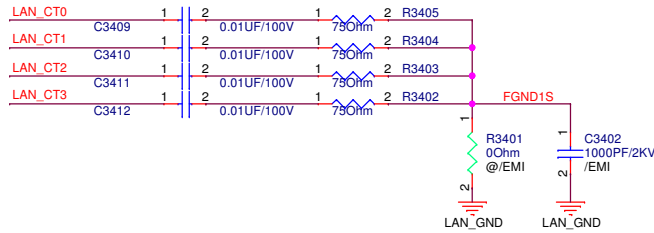
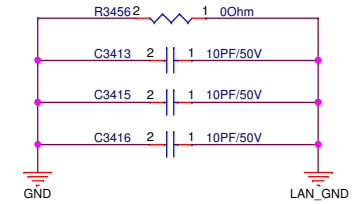
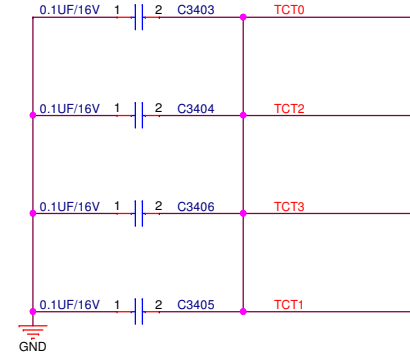




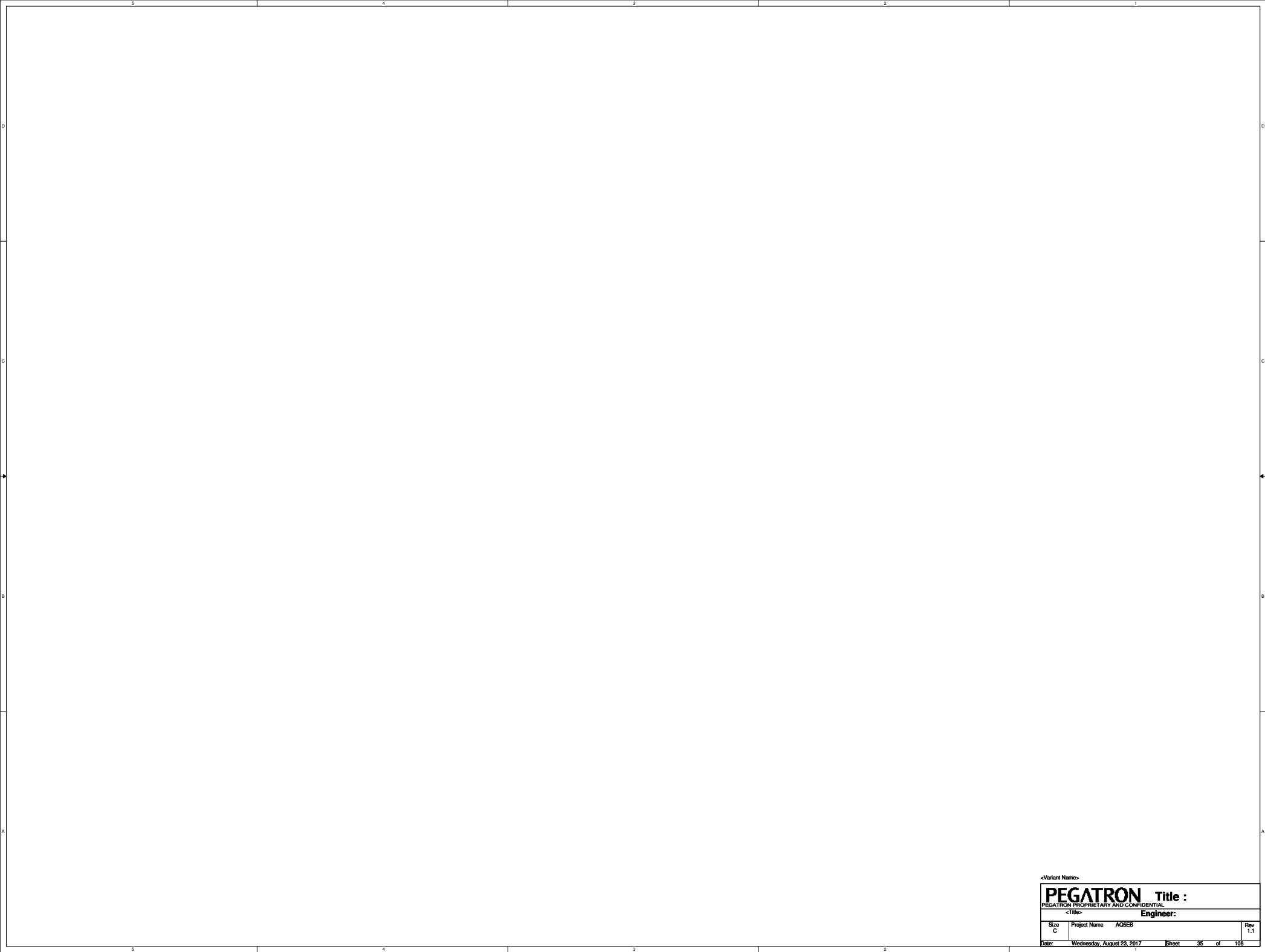




+3VSUSO +3VSUS 4,24,25,26,28,30,31,33,42,51,53,62,67,68,81,92

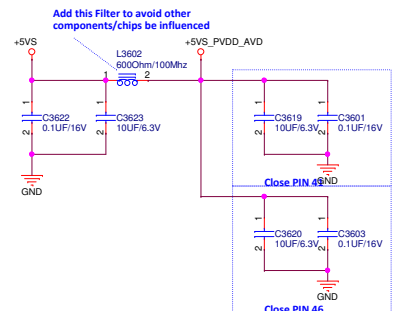
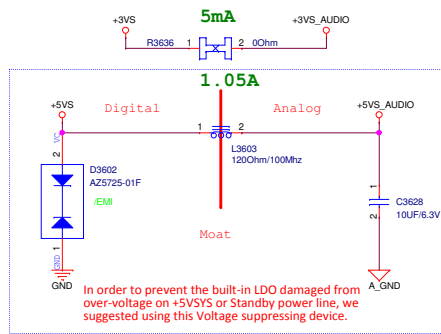
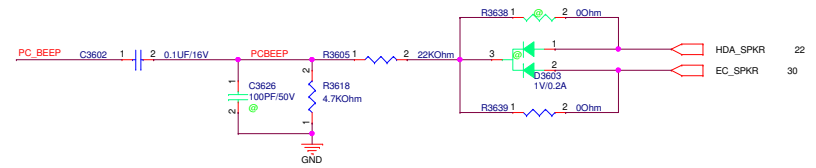
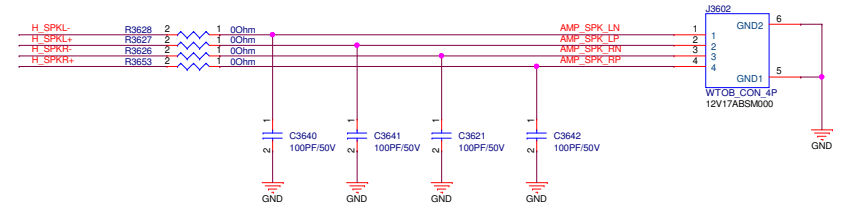
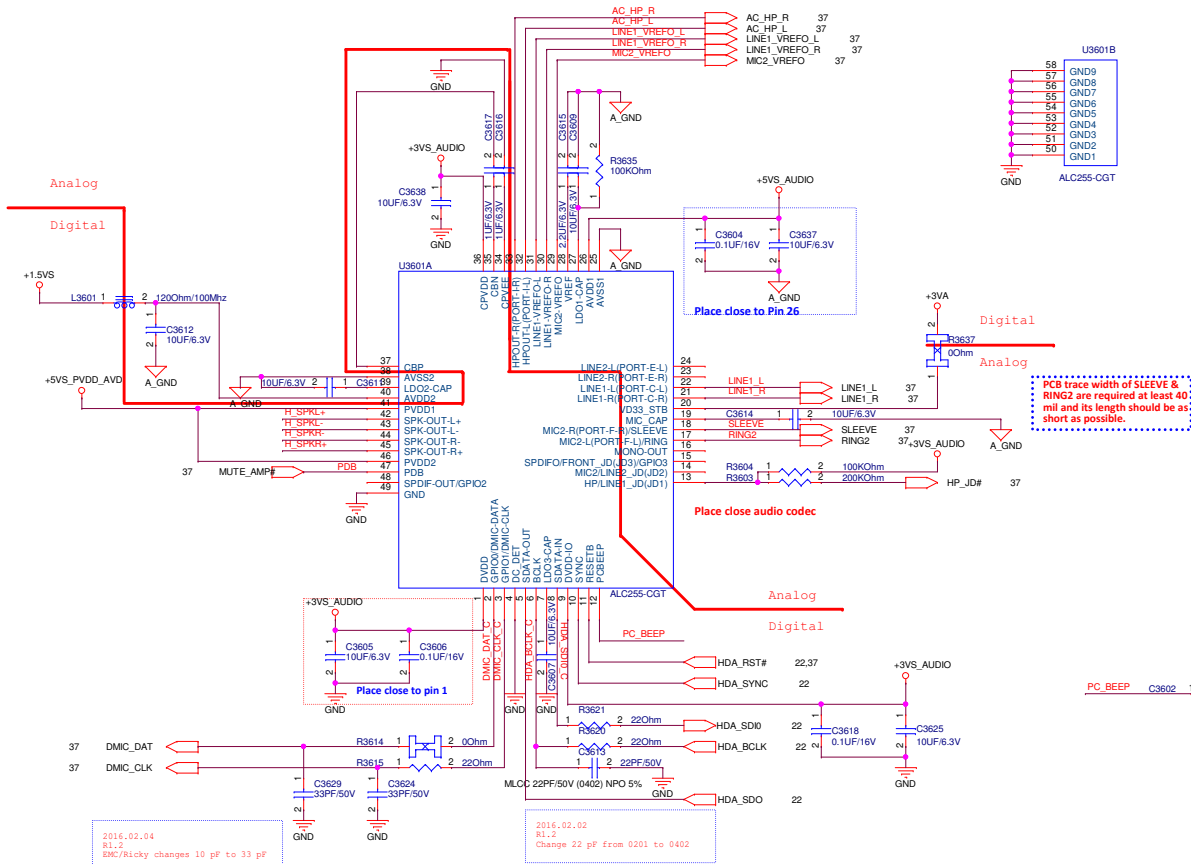


Place near chassis GND



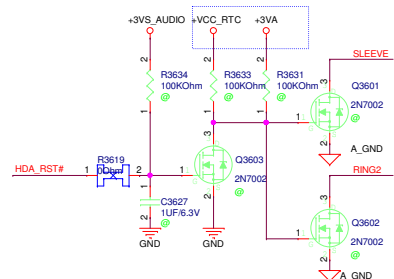
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AQSEB		Rev 1.1
Date: Wednesday, August 23, 2017		Sheet	35 of 108

## AUD\_ALC255

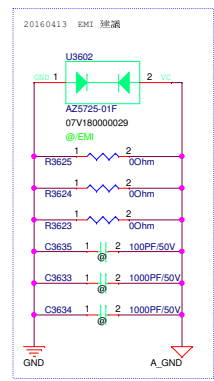


**<<Attention>>**  
**For power\_on/off de-pop circuit and system booting warning signal:** Please System BIOS Engineer Note :  
 1. If you want the system make warning signal after power on , please let EC\_MUTE# High.  
 2. If your design want to system make warning signal, for example NO CPU or Memory installation or Bad BIOS, please change to OR Gate or contact our local FAEs for more details about the control circuit

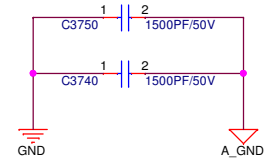
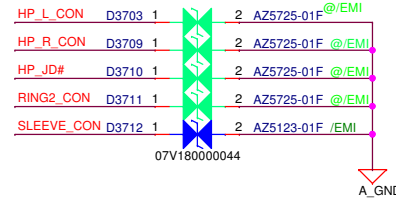
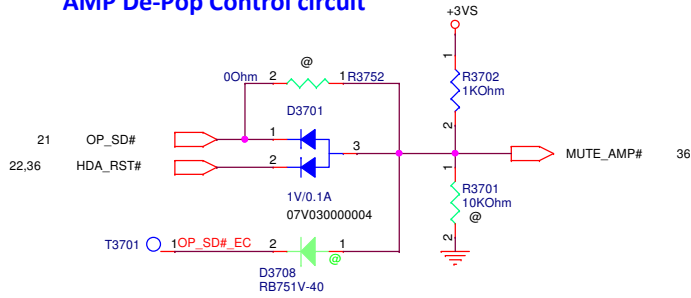
### Grounding circuit for combo jack SLEEVE pin



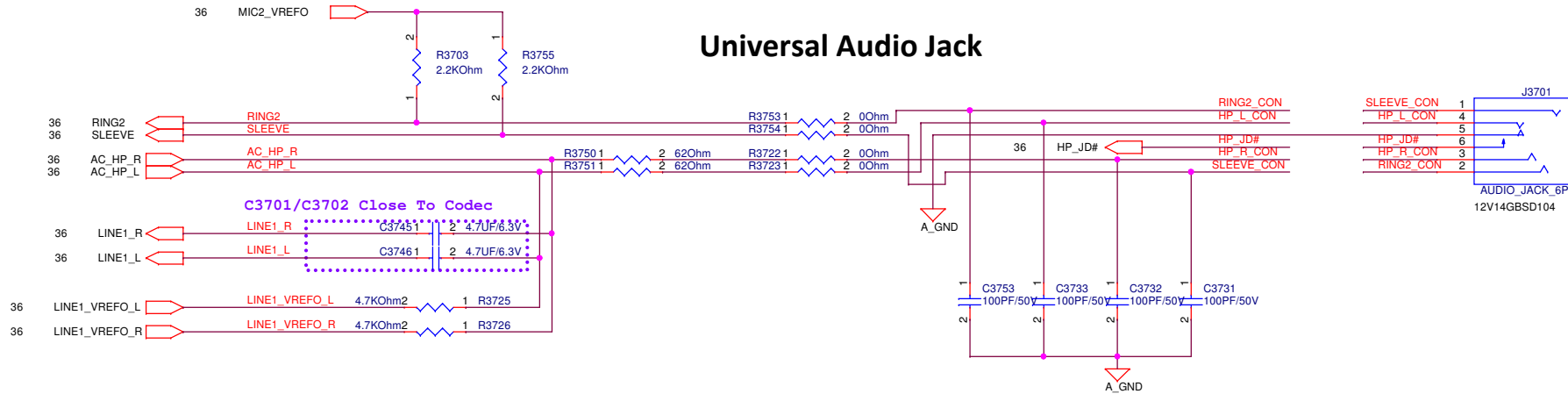
To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power.



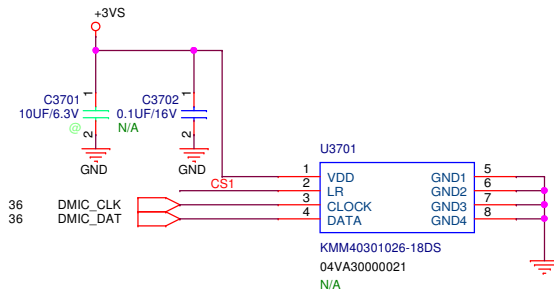
## AMP De-Pop Control circuit



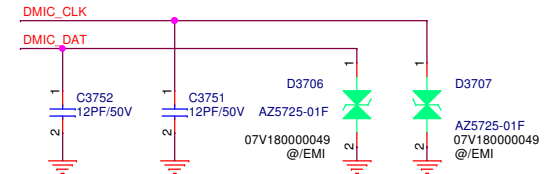
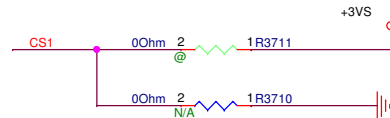
## Universal Audio Jack



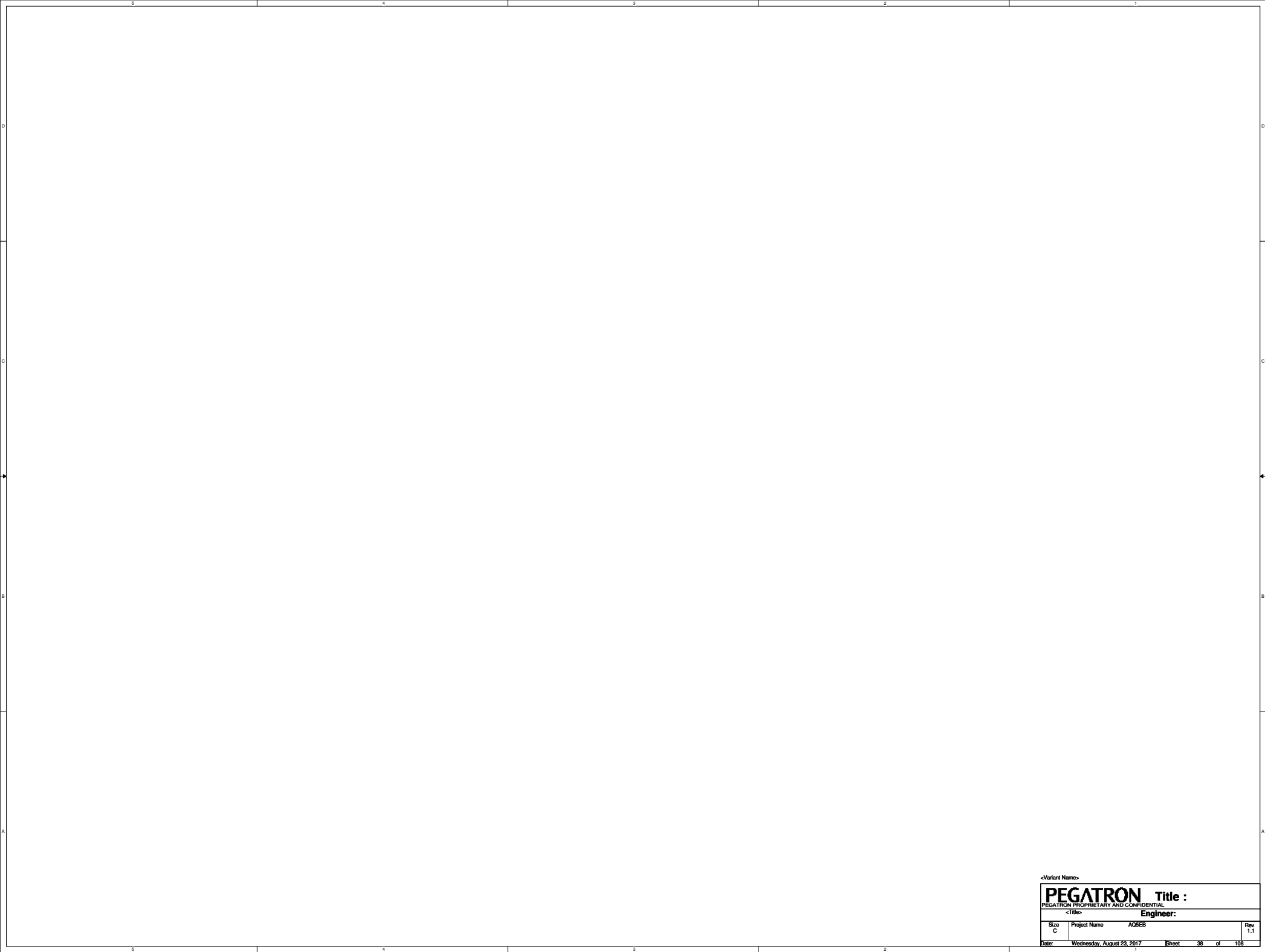
## DMIC



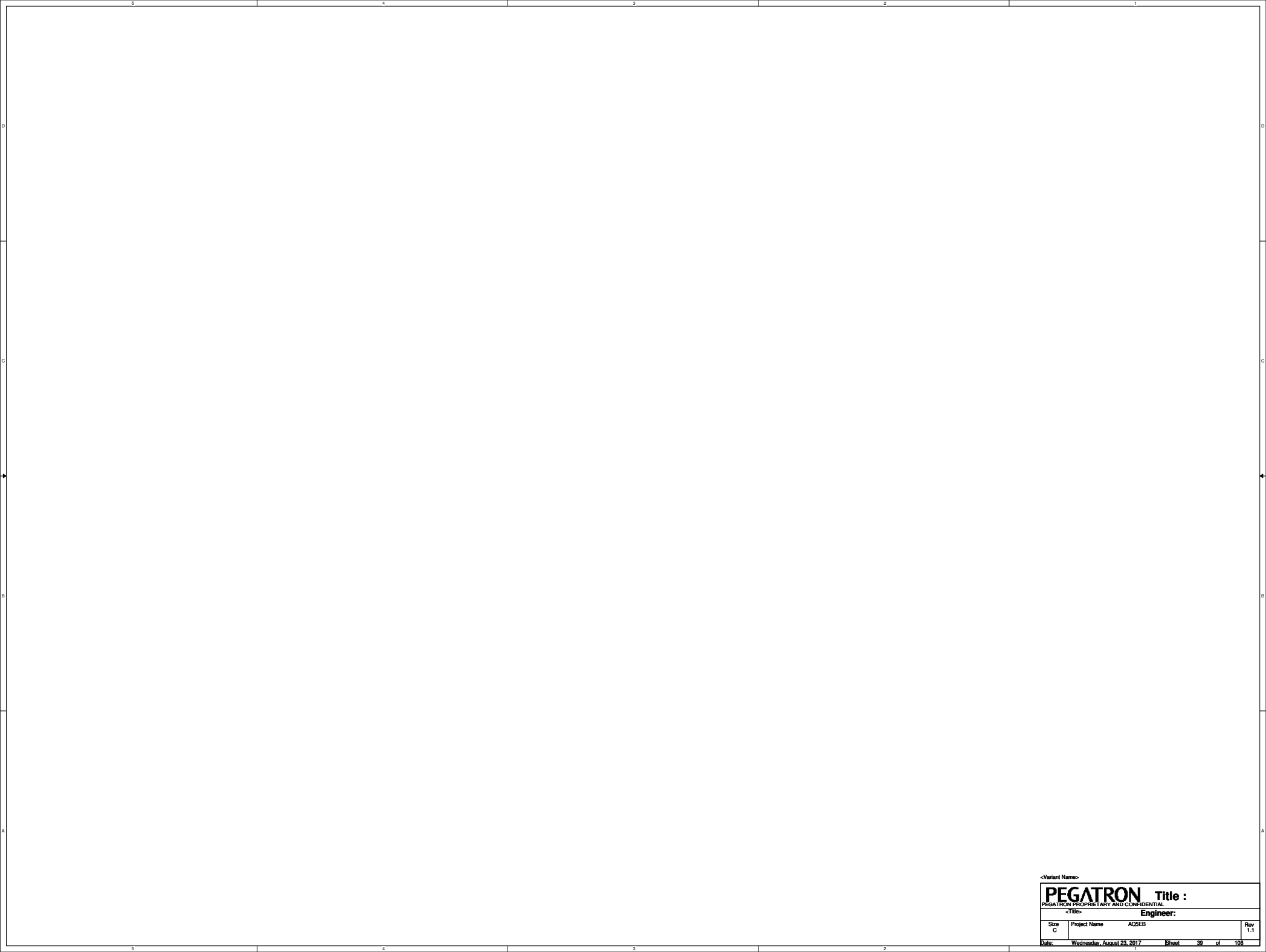
Single MIC	Left Channel	Right Channel
CS Pin	Pull Down	Pull Up



<Variant Name>



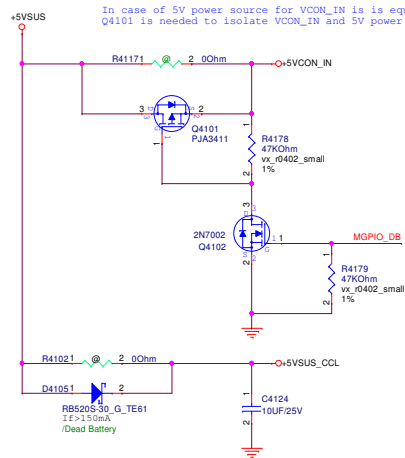
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AQ5EB	Rev 1.1	
Date: Wednesday, August 23, 2017		Sheet 38 of 108	



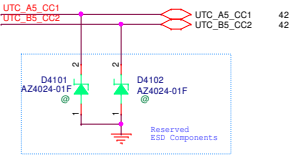
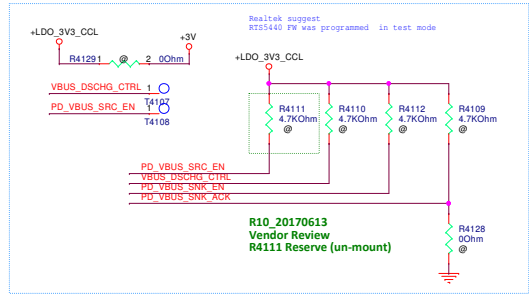
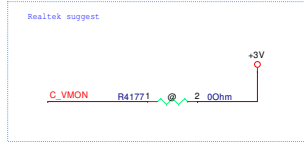
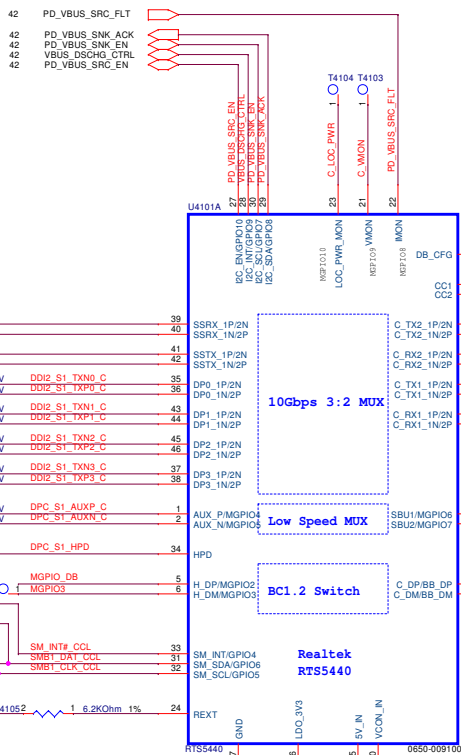
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<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AQ5EB	Rev 1.1	
Date: Wednesday, August 23, 2017		Sheet 39 of 108	



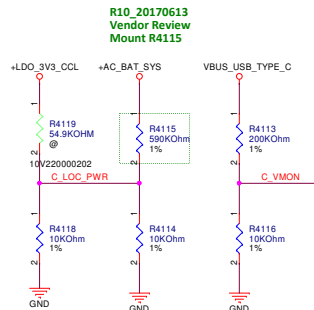
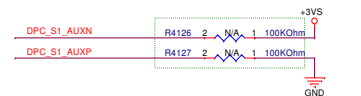
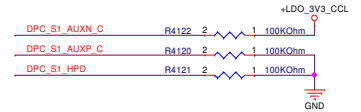
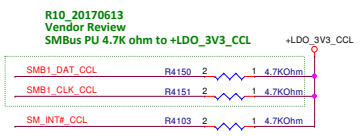




	VBUS_DSCHG	SRC_PS_EN	SRC_PS_FLT	SNK_PS_EN	SNK_PS_ACK
5440	GP109/ MSP102	GP1010	MSP108	GP107/ MSP103	GP108/ MSP101



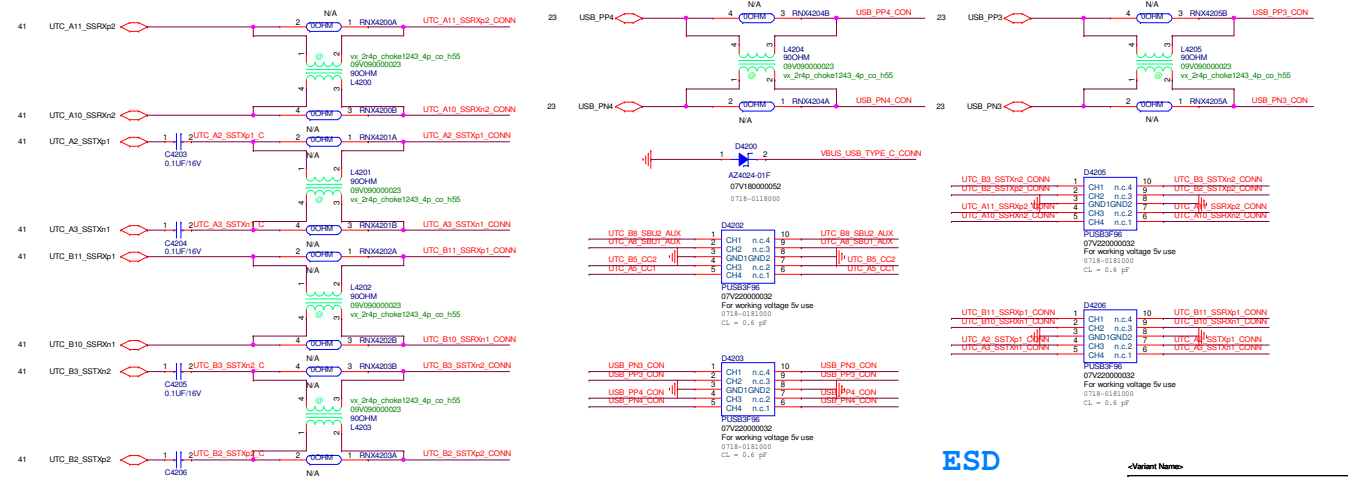
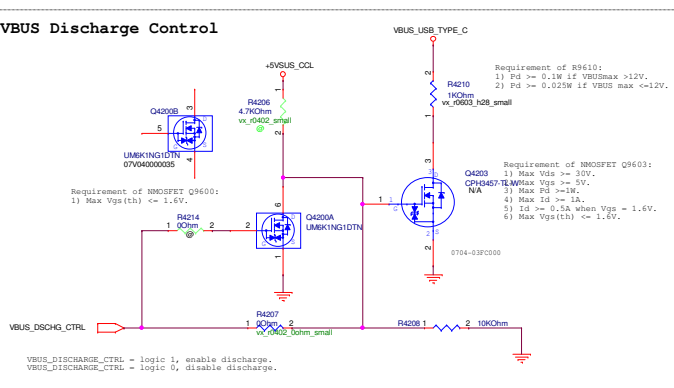
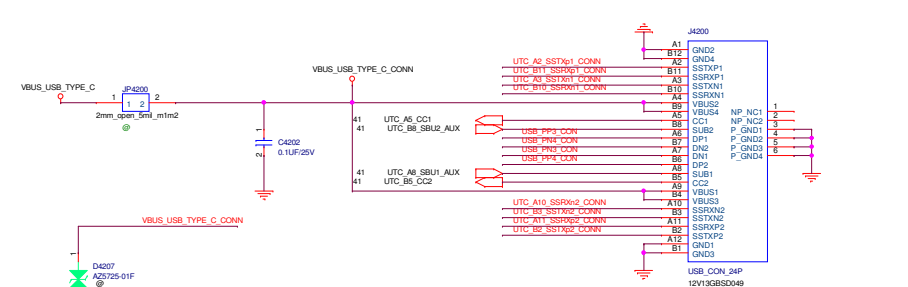
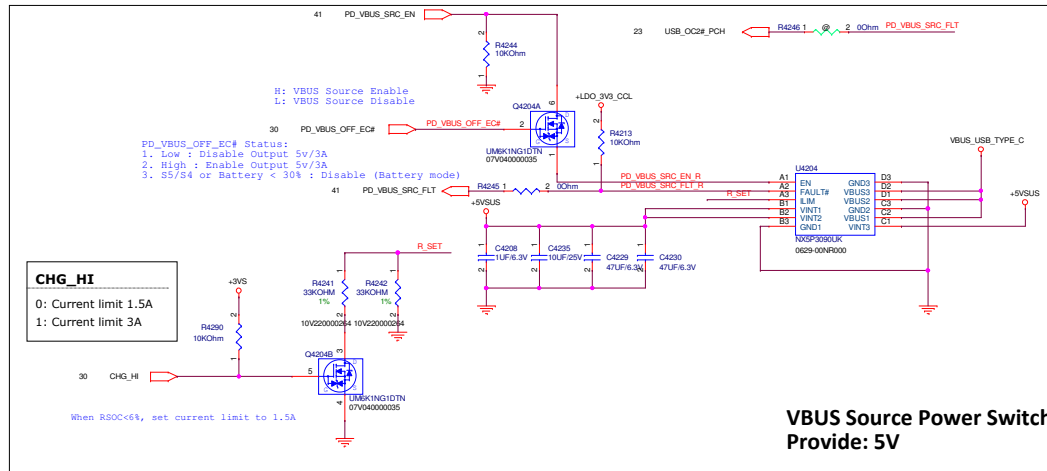
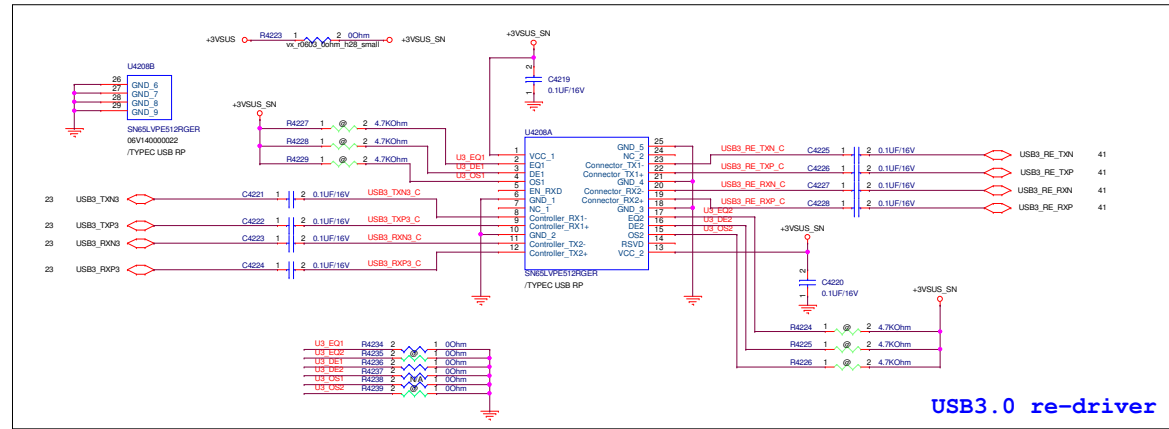
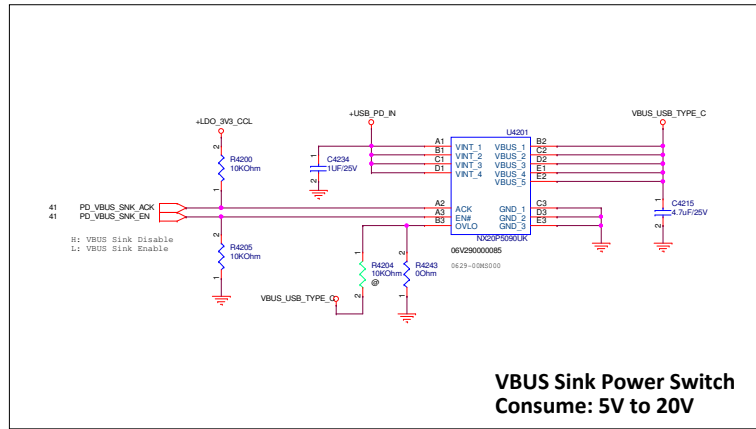
NOTE:  
1.If the 5V\_IN power supply voltage is fixed 5V or variable from 3.3V to 5V. Remove the 0ohm resistor.  
2.If the 5V\_IN power supply voltage is fixed 3.3V, stuff the 0ohm resistor



Slave Addr	R4119	R4118
0XAC	NC	10K
0XAE	54.9K	12.1K
0XB0	27.4K	15.8K
0XB2	18.2K	22.1K

R4114, R4115, R4118, R4119 must be precision resistor of 1%.

+3V 25,31,44,57,67,82,91  
+5VSUS 42,52,56,67,81



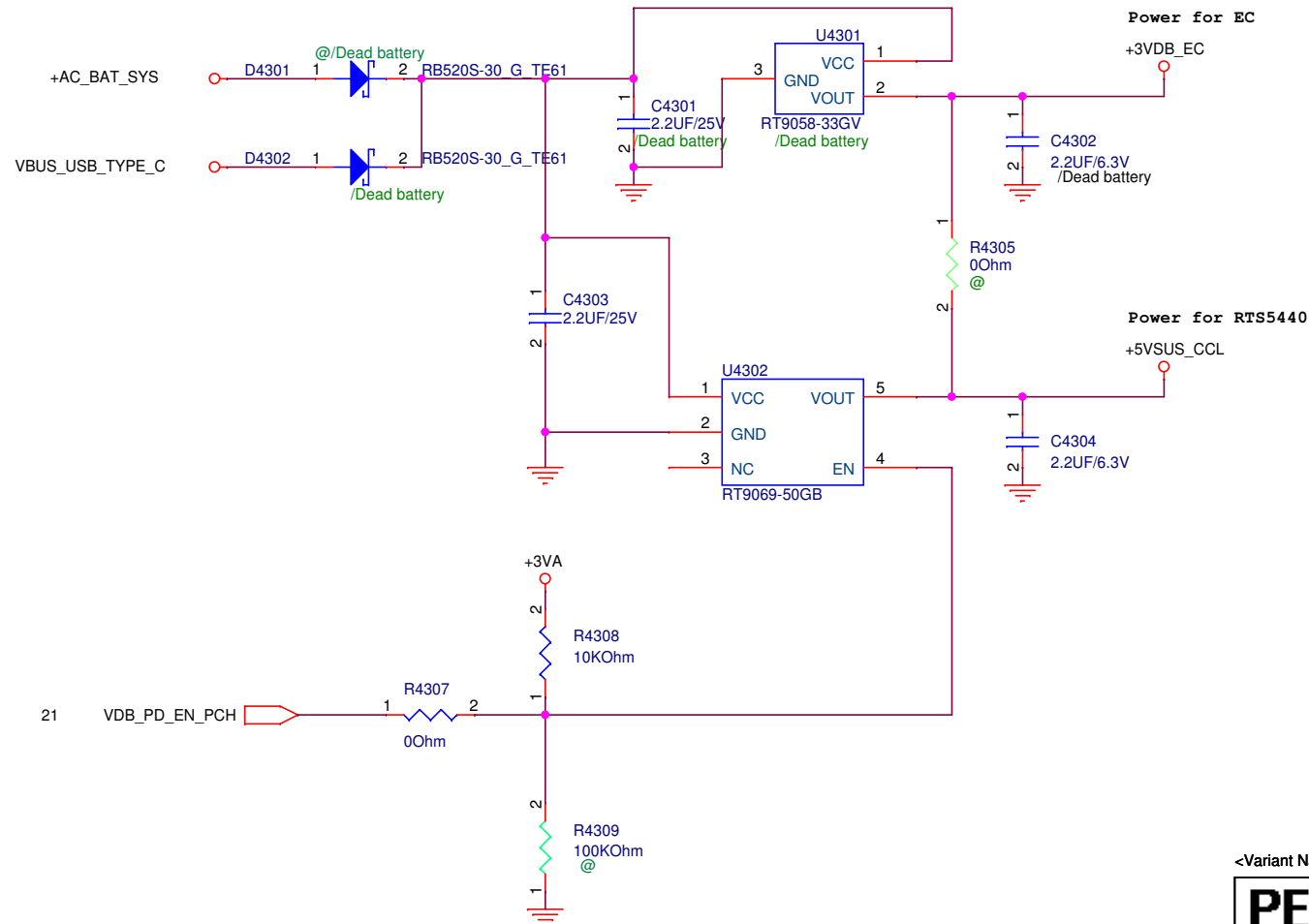
ESD

## Hardware Solution For Dead Battery

For notebook applications, if the battery charger needs higher voltage than 5V to operate correctly, execute the steps below in the order they are listed:

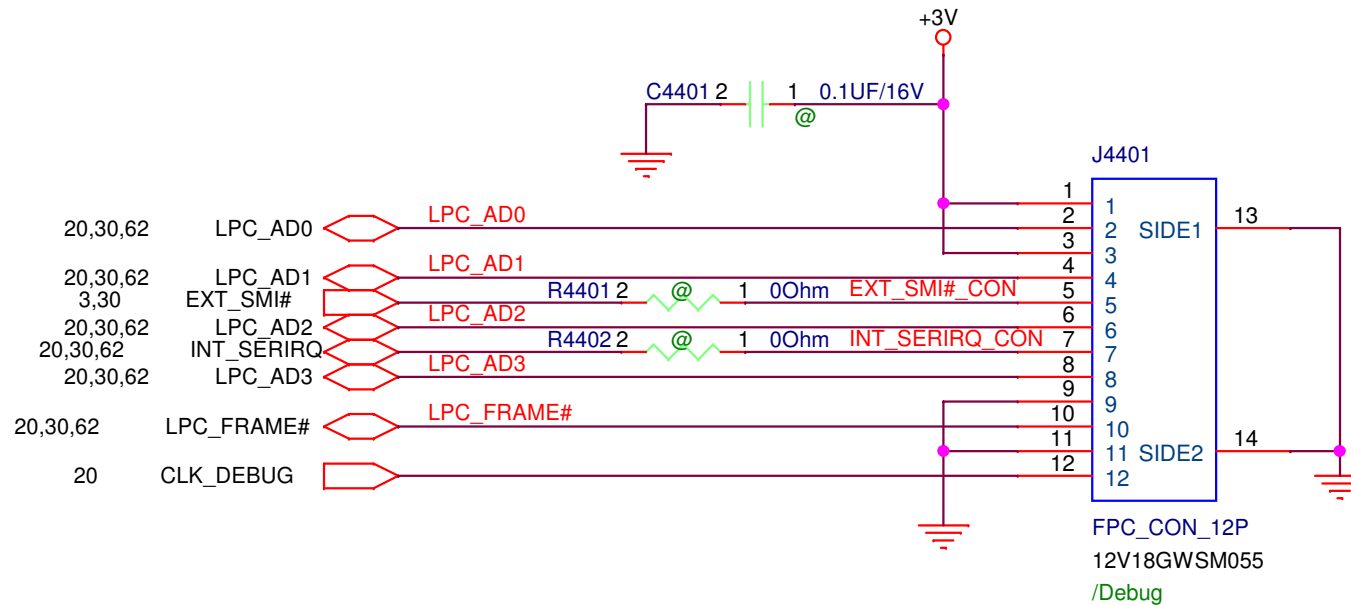
VBUS_USB_TYPE_C		VBUS_USB_TYPE_C	41,42
+AC_BAT_SYS		+AC_BAT_SYS	41,45,80,81,82,83,85,87,88
+3VDB_EC		+3VDB_EC	30
+5VSUS_CCL		+5VSUS_CCL	41,42

Requirement of U1:  
1) Vin range: 4V-30V.  
2) Vout: EC's operating voltage + Vf of D1  
3) Output current >= EC's operating current.



<Variant Name>

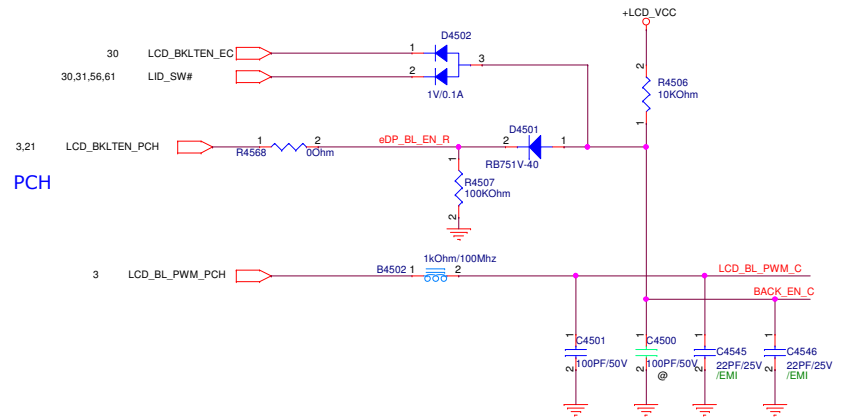
<b>PEGATRON</b>		Title : <b>Dead Battery</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: <b>Bill Yang</b>	
Size <b>Custom</b>	Project Name <b>AQ5EB</b>		Rev <b>1.0</b>
Date: <b>Wednesday, August 23, 2017</b>	Sheet	<b>43</b>	of <b>97</b>



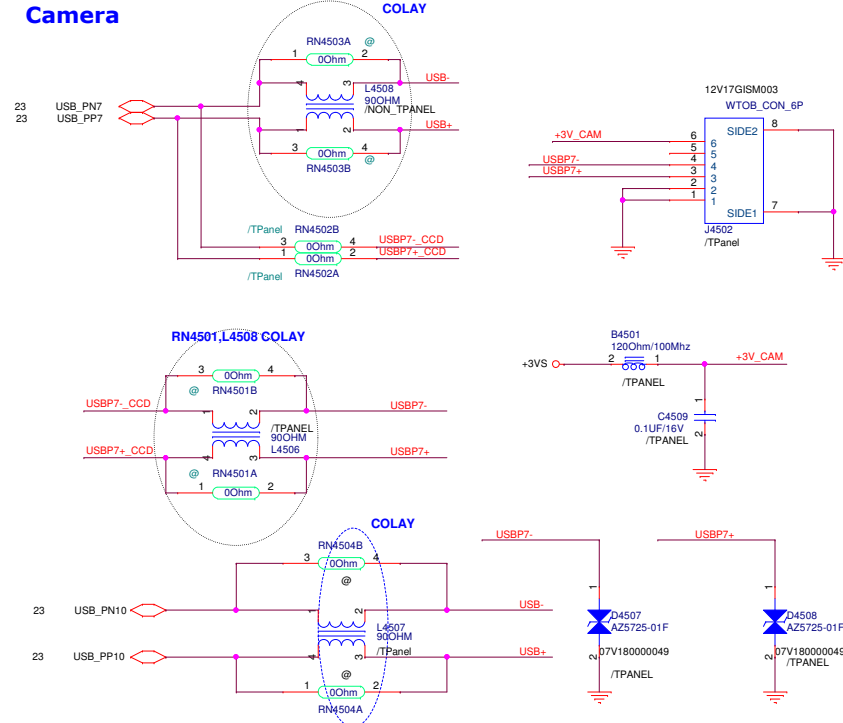
<Variant Name>

<b>PEGATRON</b>		Title : <b>BUG_Debug</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <b>Bill Yang</b>	
Size Custom	Project Name <b>AQ5EB</b>		Rev 1.0
Date: <b>Wednesday, August 23, 2017</b>		Sheet <b>44</b> of <b>108</b>	

Controller circuit



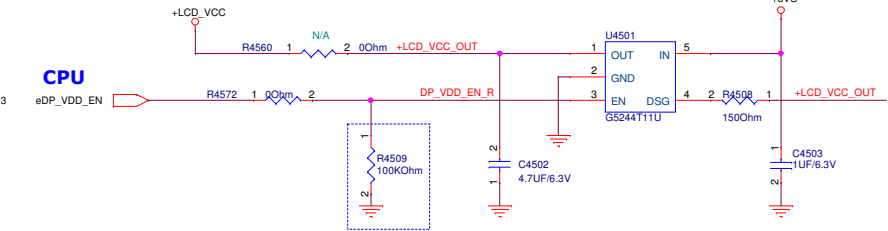
Camera



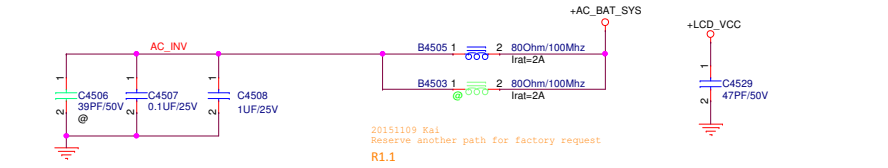
eDP HPD



LCD\_VCC for eDP

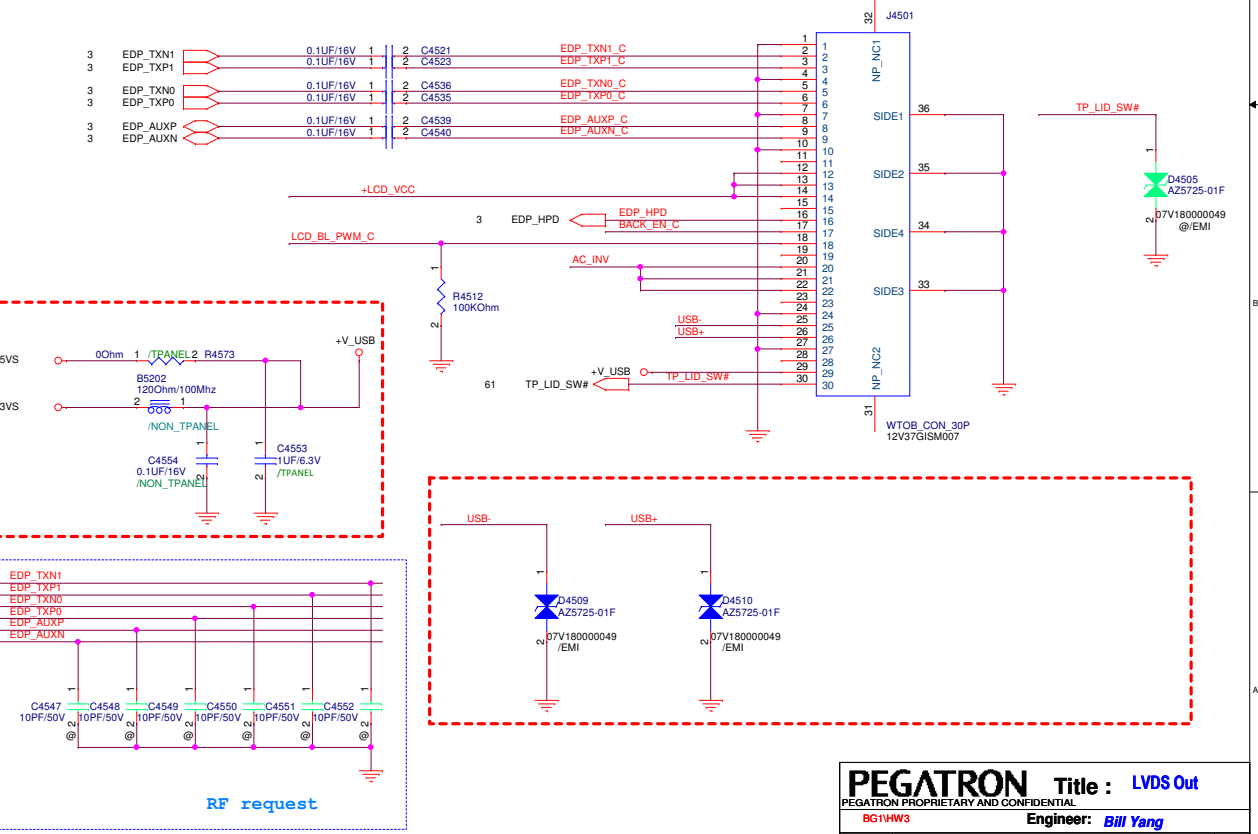


Check PCH/FCH or CPU PD

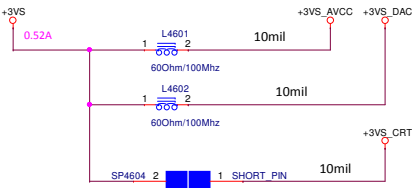


eDP Connector

NOTE:  
Entire trace of Panel\_VCC & LCD\_VCC should be wider than 80-mil

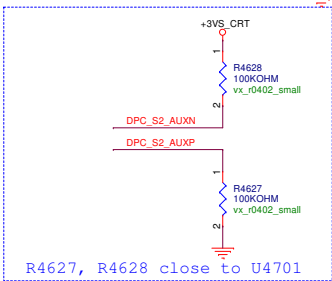
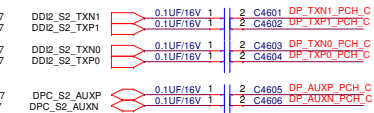


Power



CPU Interface

DP main link total length < 8 inch  
VIA < 2



Rom / Flash Mode :

	POL1 (Pin10)	
	0	1
POL2 (Pin9)	0	No Use
	1	(V) Rom mode
		Ext Flash mode

Embedded EDID setting :

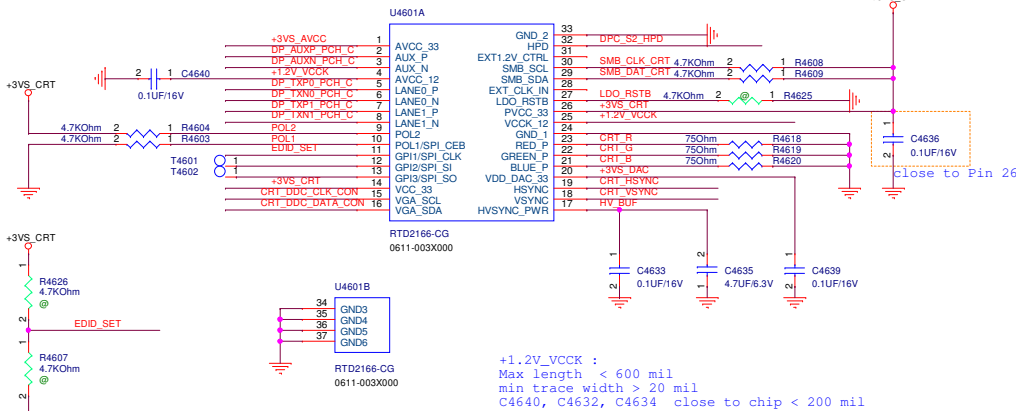
EDID_SET (Pin11)	Mode
0 or NC	(V) Disable RTD2166 Embedded EDID
1	Enable RTD2166 Embedded EDID

LDO Mode :

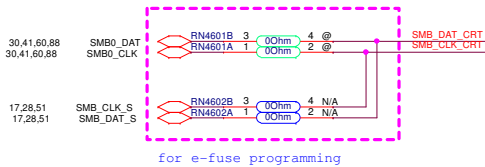
LDO_RSTB (Pin27)	Mode
1 or NC	(V) embedded LD0 Mode
0	External 1.2V Mode

1: Pull High    0: Pull Down

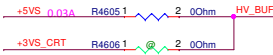
DP2VGA Realtek RTD2166



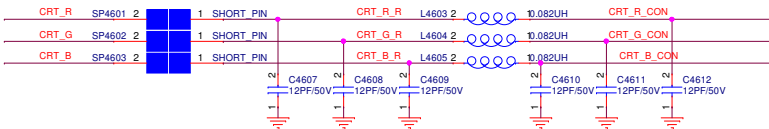
+1.2V\_VCC :  
Max length < 600 mil  
min trace width > 20 mil  
C4640, C4632, C4634 close to chip < 200 mil



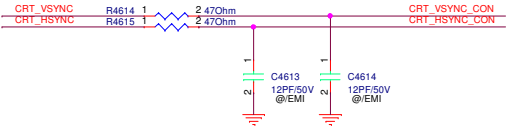
CRT\_HV Sync Voltage setting :  
R4605 : 5V  
R4606 : 3.3V



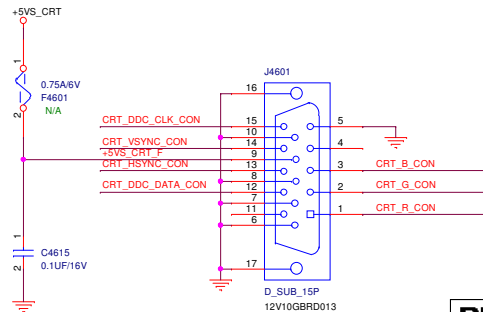
Max mismatch between RGB signal < 200 mil,  
total trace length < 6 inch



CRT\_HV Sync total trace length < 6 inch

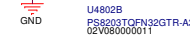


D-SUB Connector





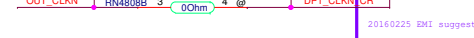
## HDMI



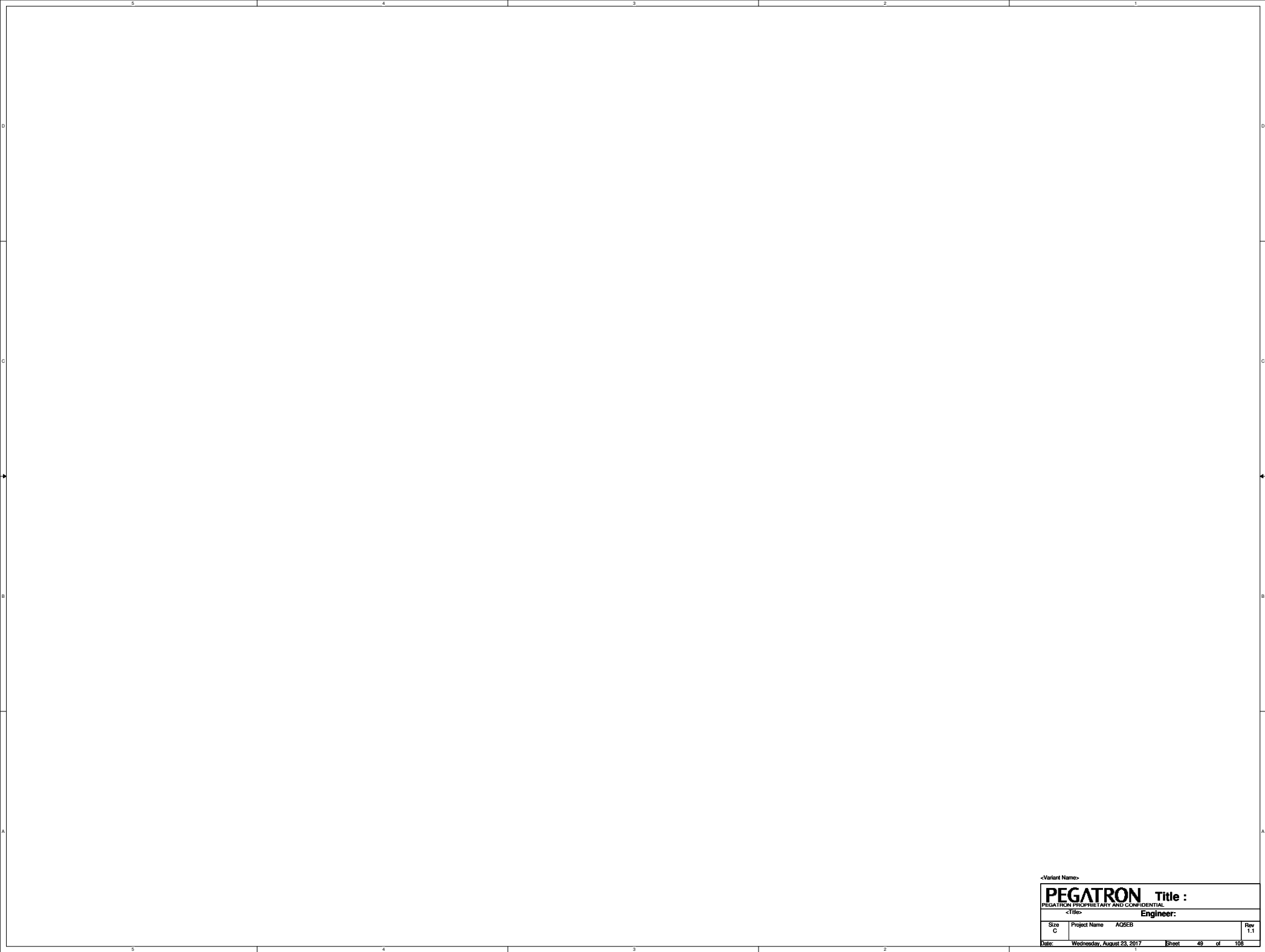
```

DCIN EN : DC coupling enable; Internal pull down at ~150k $\Omega$ , 3.3V I/O.
L: default, AC coupling input
H: DC coupling input
PRE : Output pre-emphasis setting; Internal pull down at ~150k $\Omega$ , 3.3V
I/O.
L: no pre-emphasis
H: 2.5dB pre-emphasis
EQ : Receiver equalization setting; Internal pull down at ~150k $\Omega$ , 3.3V
I/O.
L: programmable EQ for channel loss up to 12.4dB @ 3Gbps
H: programmable EQ for channel loss up to 4.3dB @ 3Gbps
M: programmable EQ for channel loss up to 8.6dB @ 3Gbps

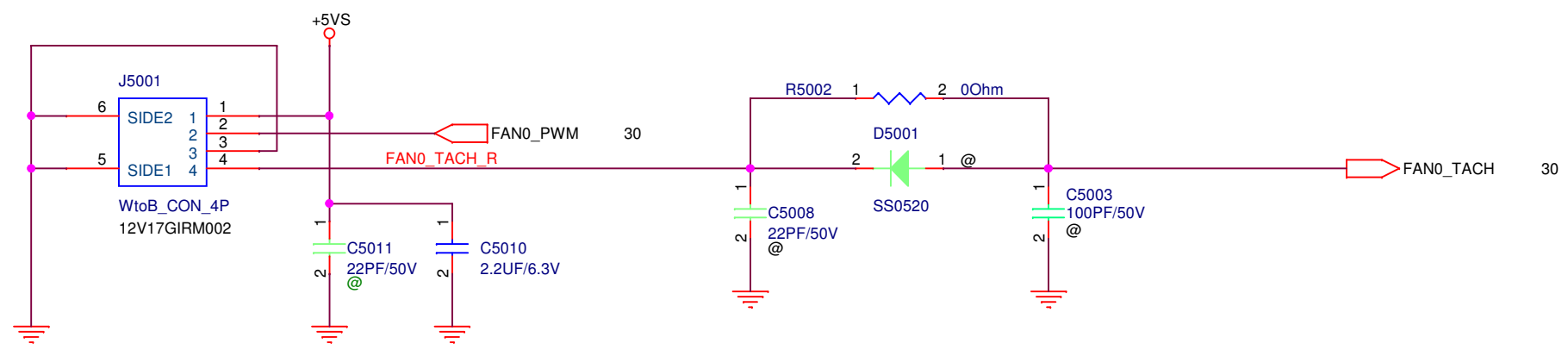
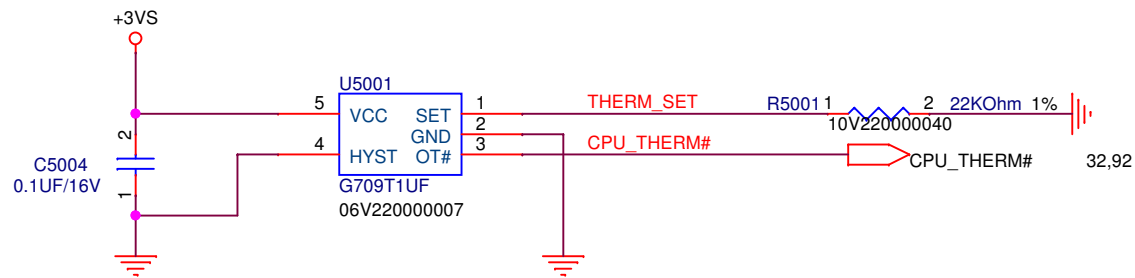
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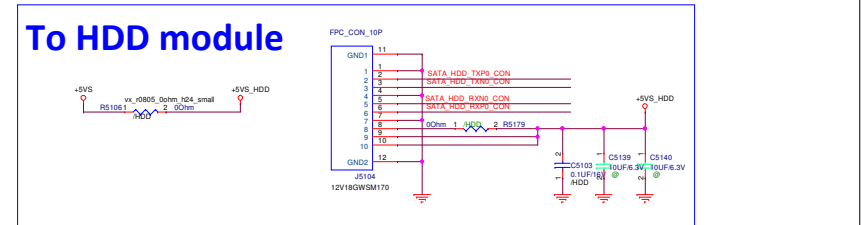
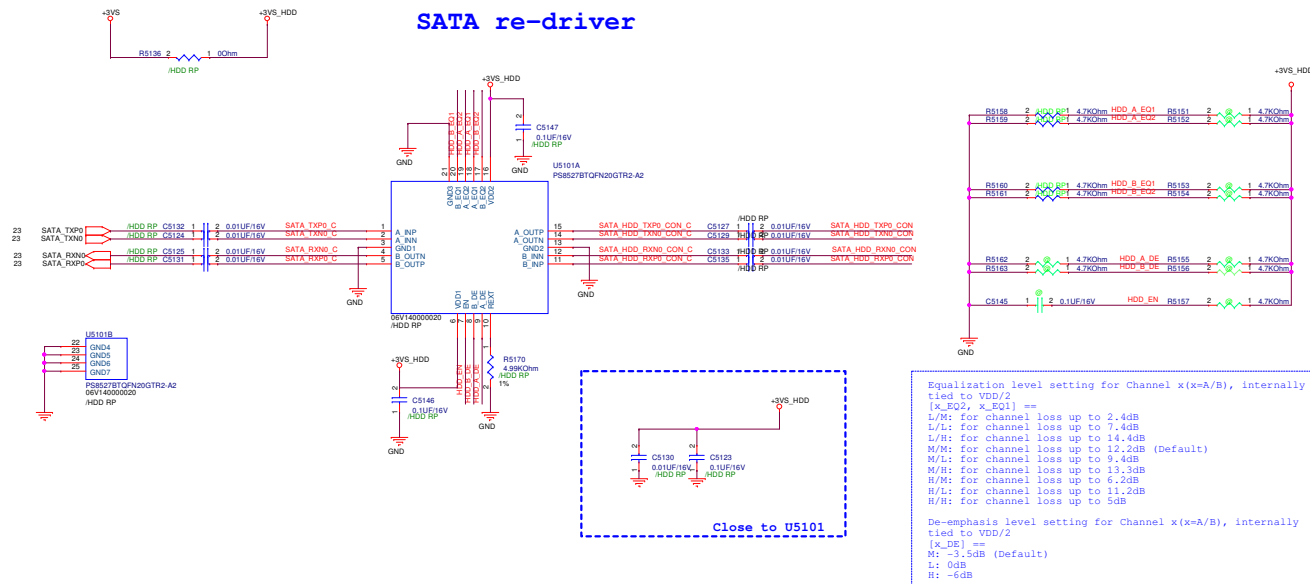




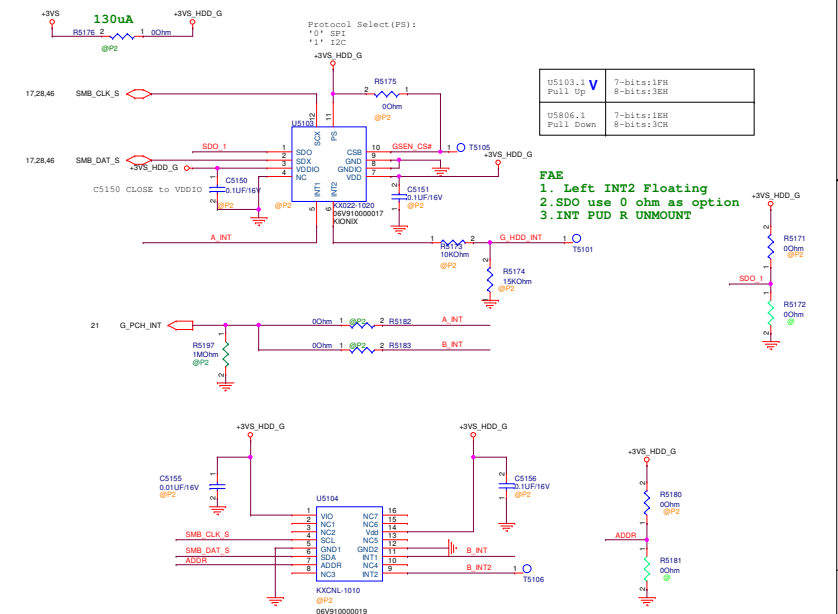
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AQSEB		Rev 1.1
Date: Wednesday, August 23, 2017		Sheet	49 of 108



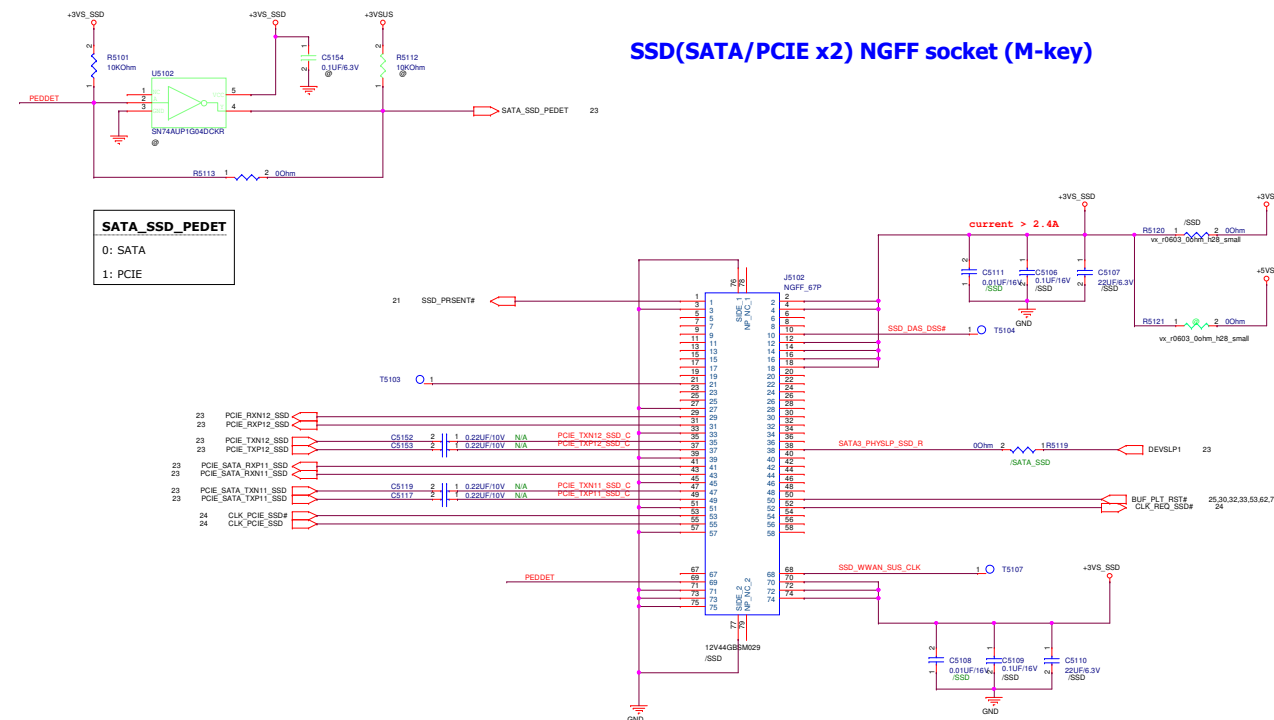
## HDD



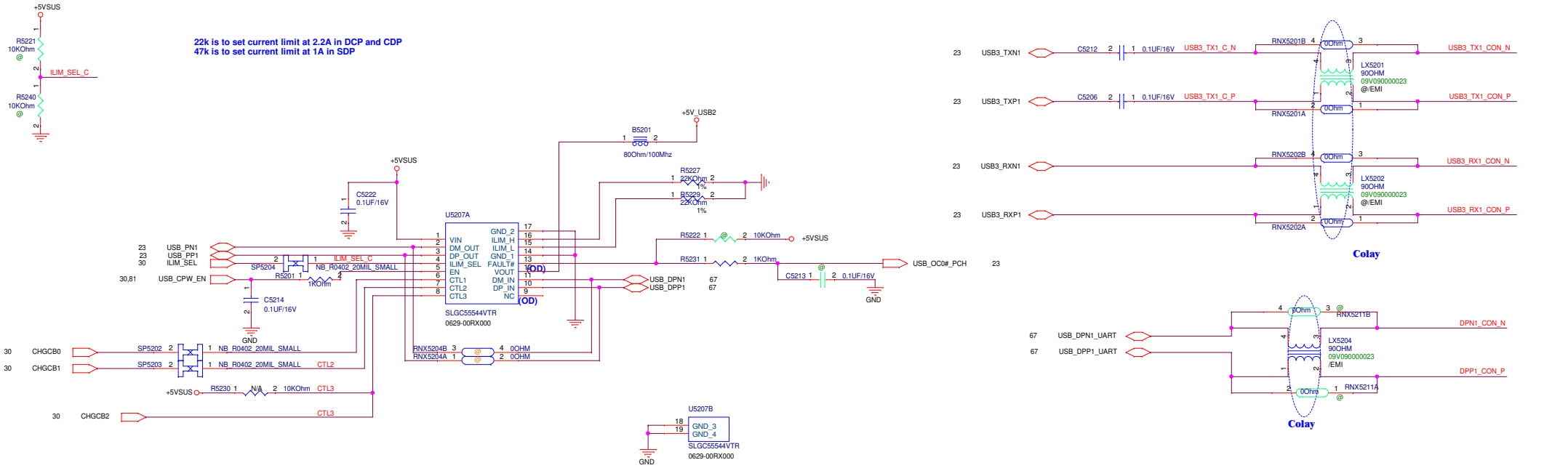
## HDD G-Sensor



## SSD(SATA/PCIE x2) NGFF socket (M-key)

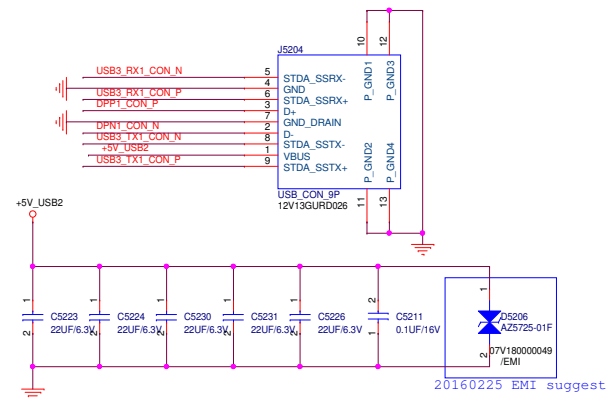
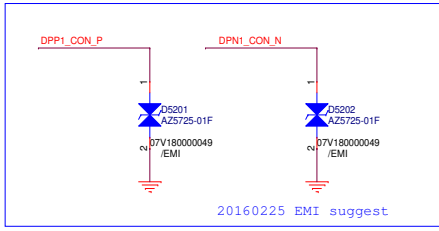
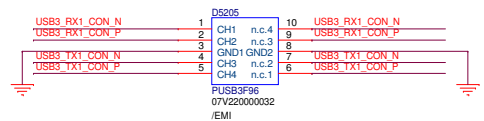


USB 3.0 ports x 1 with Sleep & Charge Left\_Down  
TPS2544 Device True Table



System Global Power State	TPS2544 Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S0	SDP (Standard Downstream)	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S3/S4/S5	Auto mode, no mouse wake	0	0	1	0	ILIM_HI
S3	Dedicated Charging Port Auto mode, keyboard/mouse wake up	0	1	1	X	ILIM_HI
S3	SDP, keyboard/mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

PLACE ESD Diodes near USB Connector



# WLAN/ WiGig / BT

**+3V\_WLAN\_WP1 bypass capacitor:**

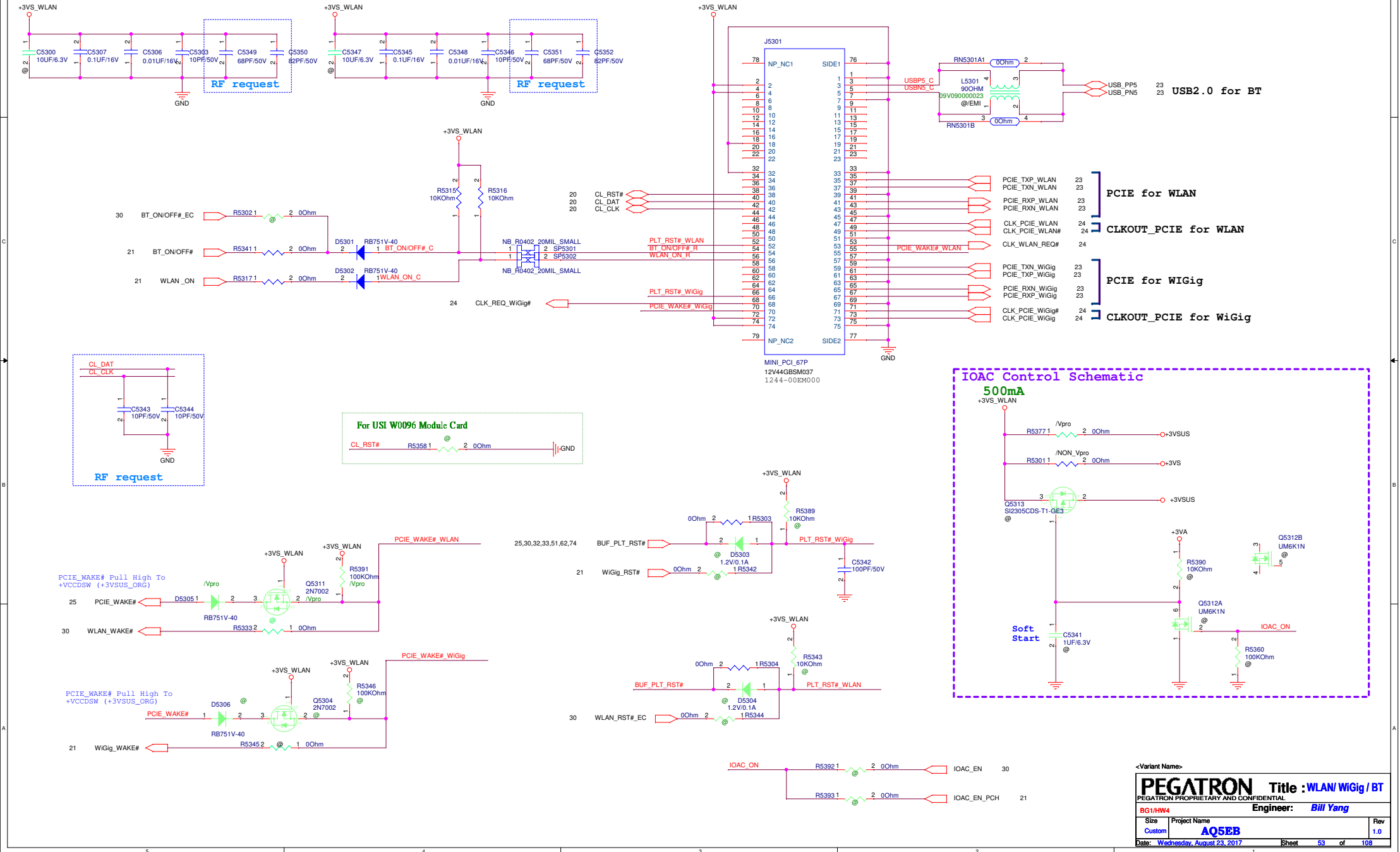
Place 0.1uF near pin 2,4

**+3V\_WLAN\_WP1 bypass capacitor:**

Place 0.1uF near pin 72,74.

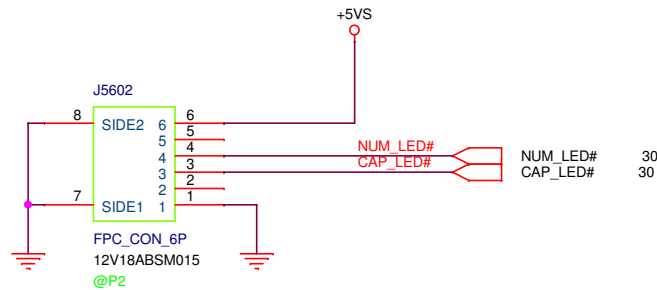
Place 10uF near +3V\_WLAN\_WP1 source side.

Place 10uF near +3V\_WLAN\_WP1 source side.





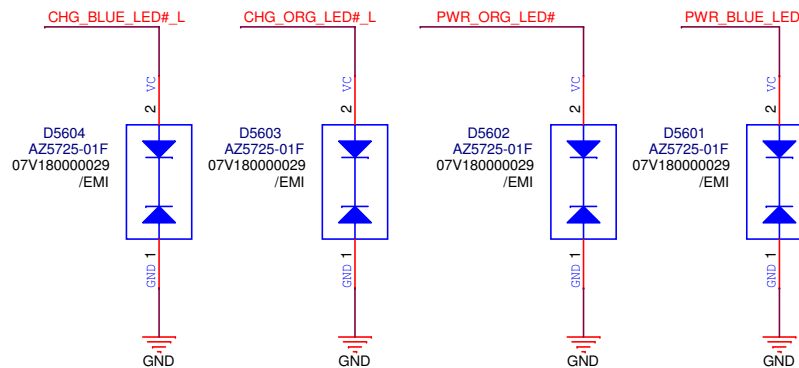
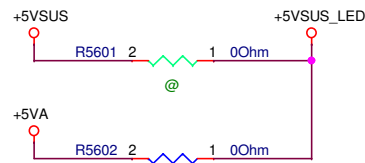
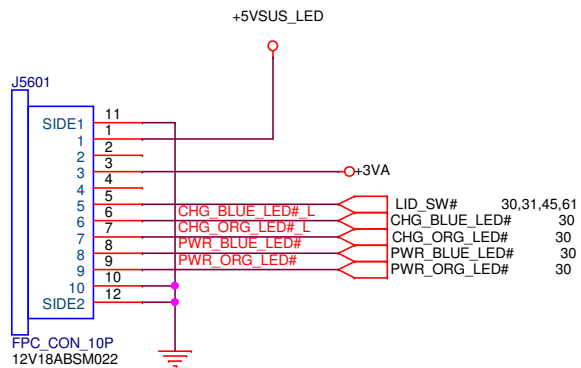




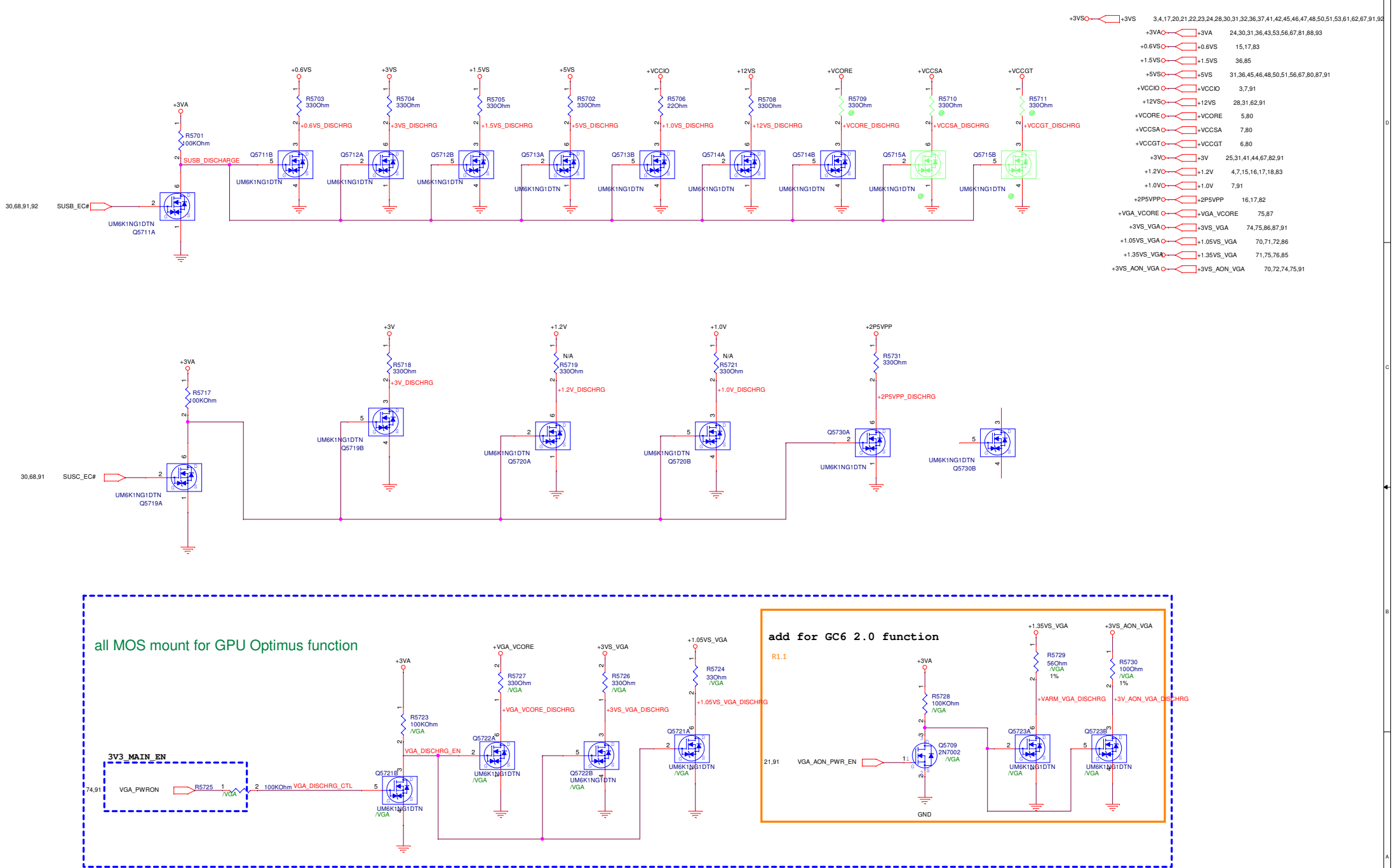
+5VS 31,36,45,46,48,50,51,57,67,80,87,91

+5VSUS 41,42,52,67,81

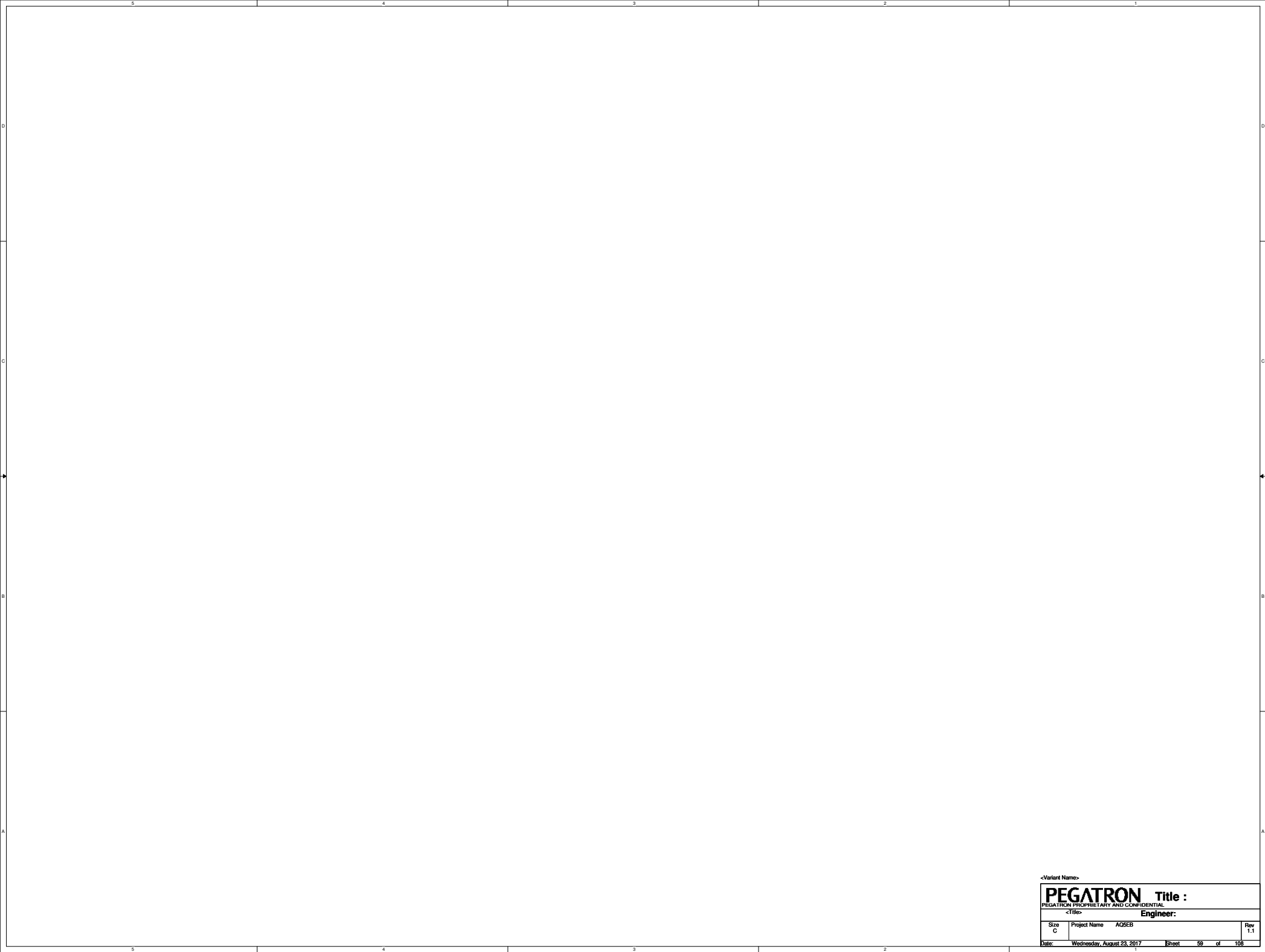
+3VA 24,30,31,36,43,53,57,67,81,88,93





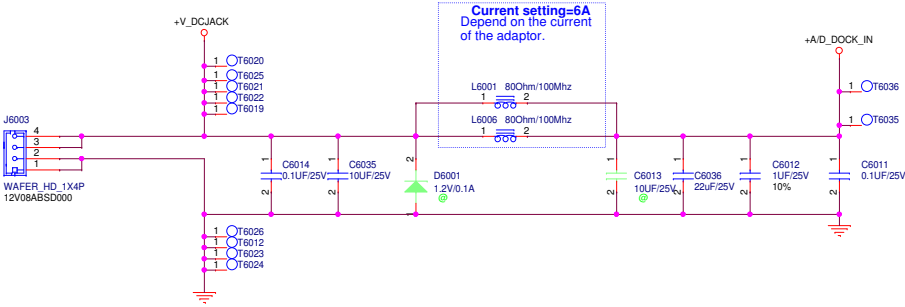






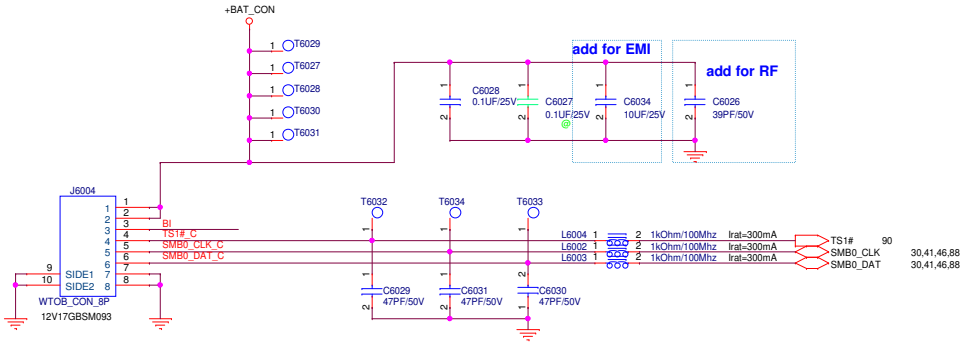
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AQSEB		Rev 1.1
Date: Wednesday, August 23, 2017		Sheet	59 of 108

DC Jack WTB CONN

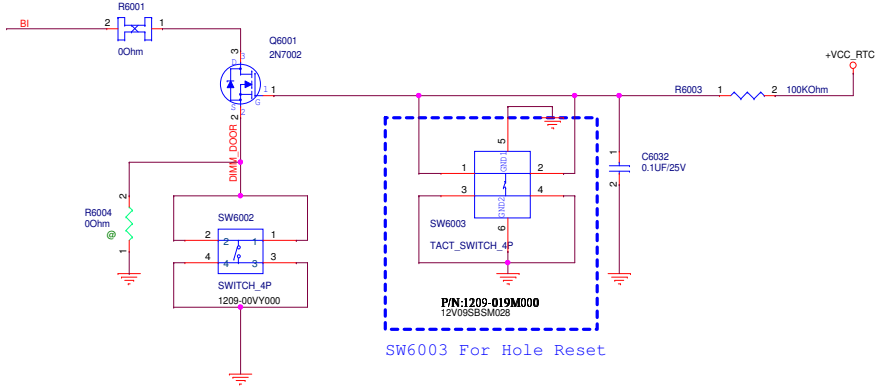


+VCC_RTC	+VCC_RTC	24,25,26,36
+3VA_EC	+3VA_EC	28,30,32
+3VA_O	+3VA	24,30,31,36,43,53,55,57,67,81,88,93
+5VA_O	+5VA	31,56,81
+1.0VSUS	+1.0VSUS	26,82
+1.8VSUS	+1.8VSUS	9,21,24,26,84
+3VSUS	+3VSUS	4,24,25,26,28,30,31,33,42,51,53,62,67,68,81,92
+5VSUS	+5VSUS	41,42,52,56,67,81
+12VSUS	+12VSUS	81,91
+3V	+3V	25,31,41,44,57,67,82,91
+12V	+12V	91
+3VS	+3VS	3,4,17,20,21,22,23,24,28,30,31,32,36,37,41,42,45,46,47,48,50,51,53,57,61,62,67,91,92
+5VS	+5VS	31,36,45,46,48,50,51,56,57,67,80,87,91
+12VS	+12VS	28,31,57,62,91
+AC_BAT_SYS	+AC_BAT_SYS	41,43,45,80,81,82,83,85,87,88
+AID_DOCK_IN	+AID_DOCK_IN	89
+BAT_CON	+BAT_CON	88
+VCCORE	+VCCORE	5,57,80
+VCCGT	+VCCGT	6,57,80
+VCCSA	+VCCSA	7,57,80
+VCCIO	+VCCIO	3,7,57,91
+RTCBAT	+RTCBAT	24

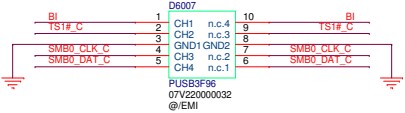
Battery Connector

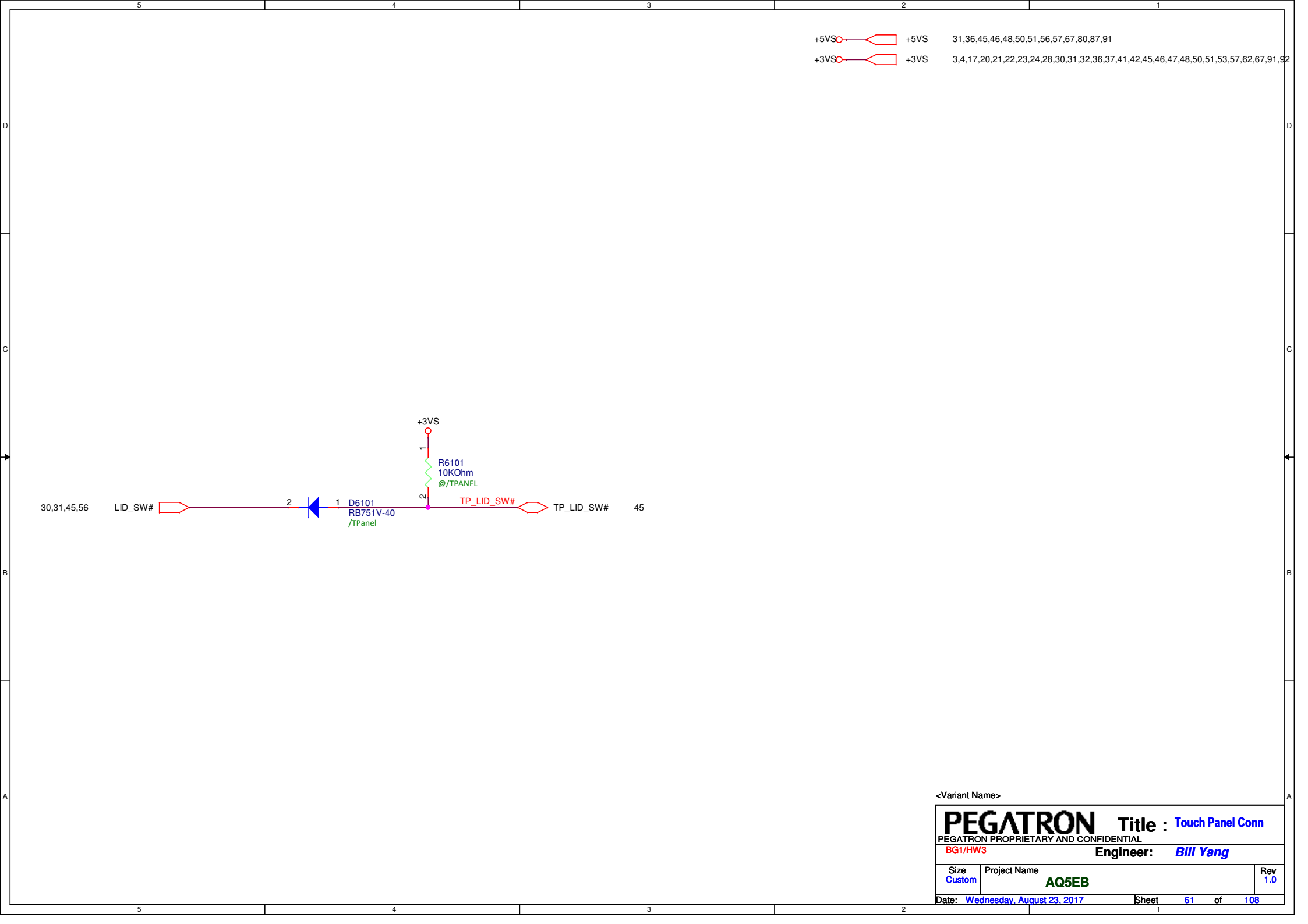


客戶提出的原因是因為若有100ohm可能會造成分壓而導致BI pin無法拉到low, 故改為0ohm

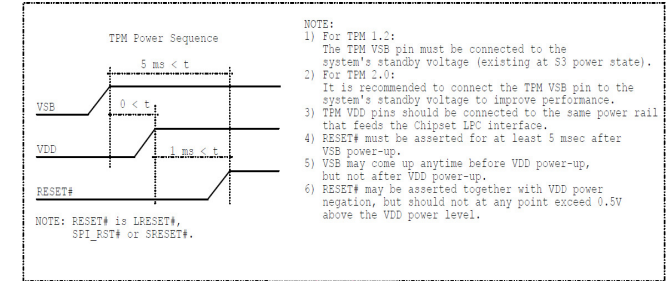
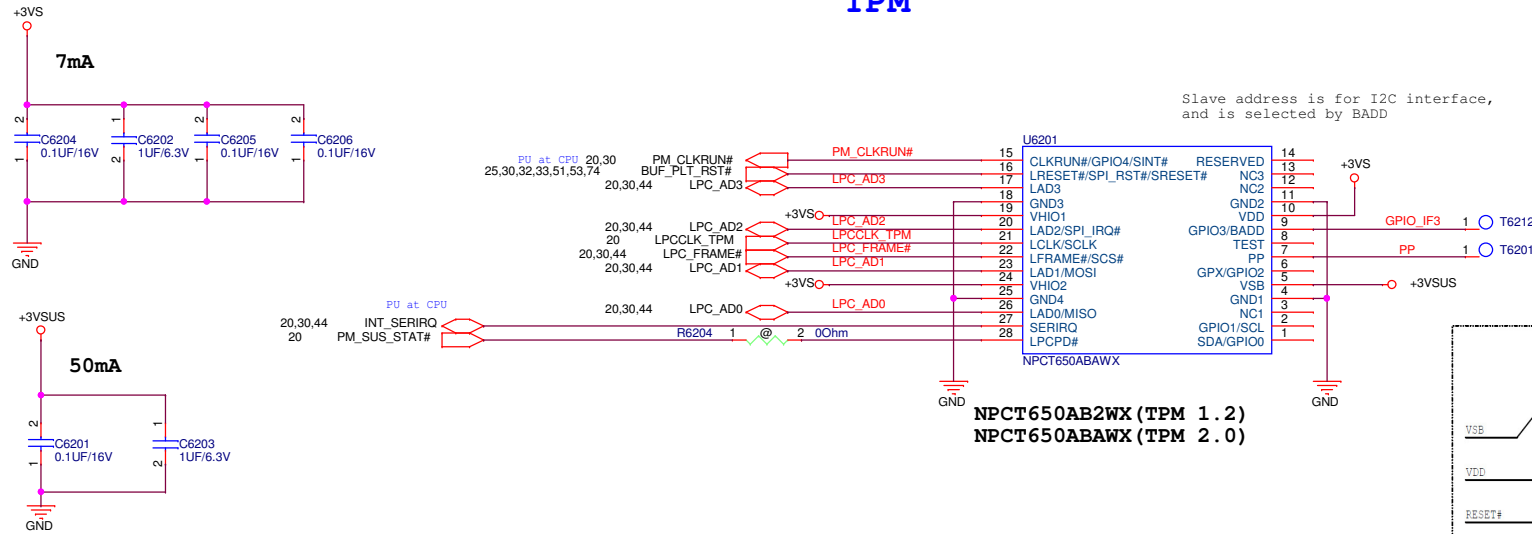


EMI 2015/10/12

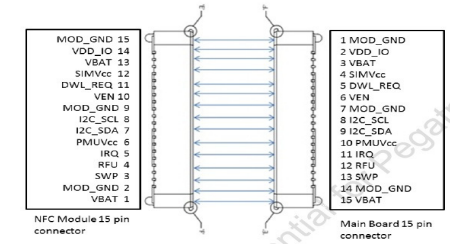
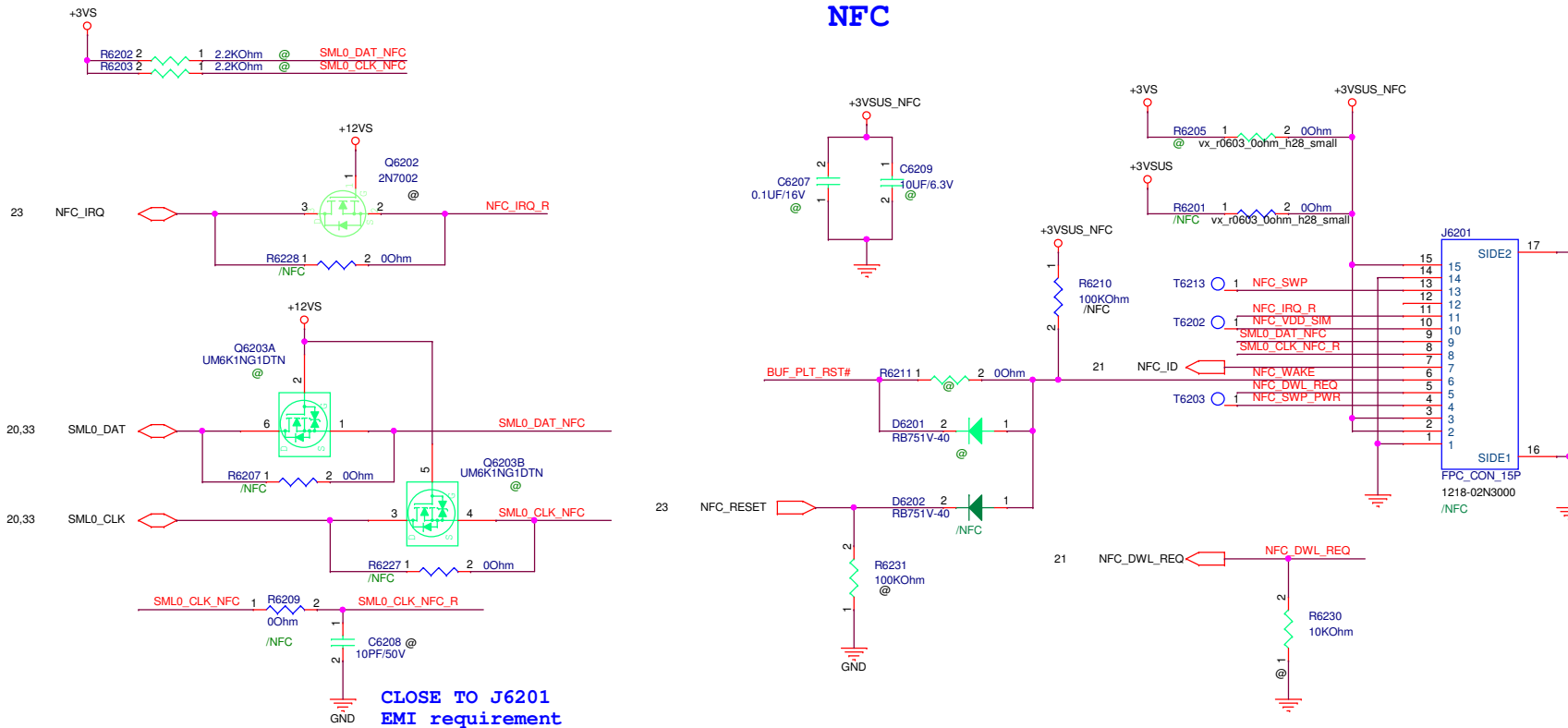




## TPM



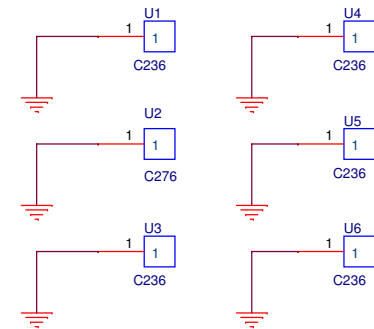
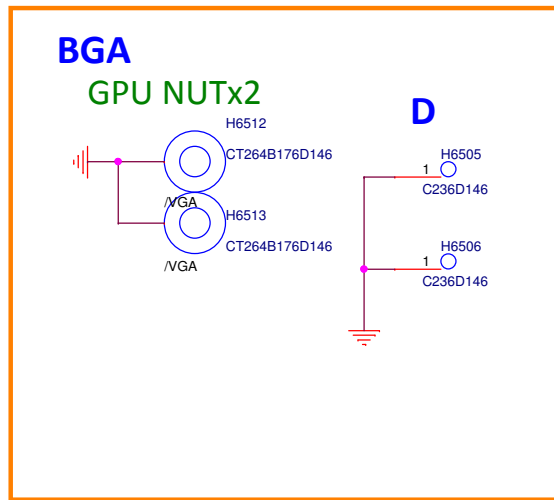
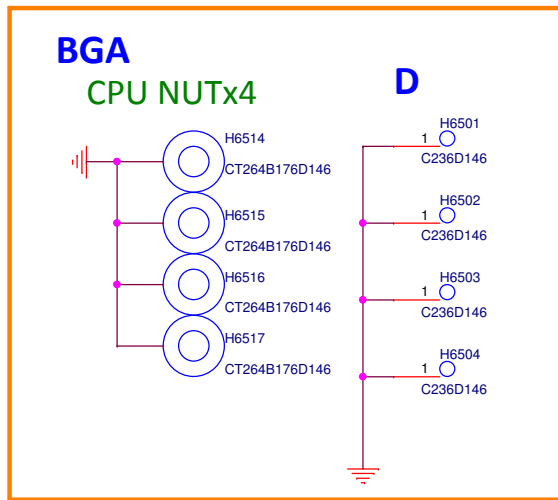
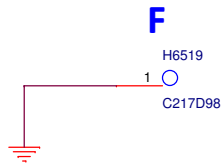
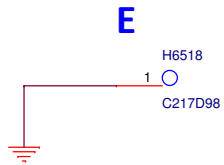
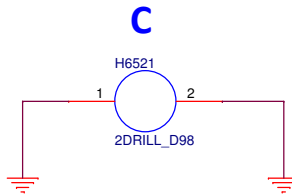
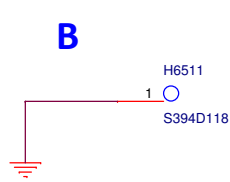
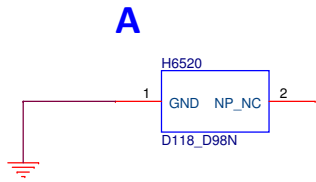
## NFC







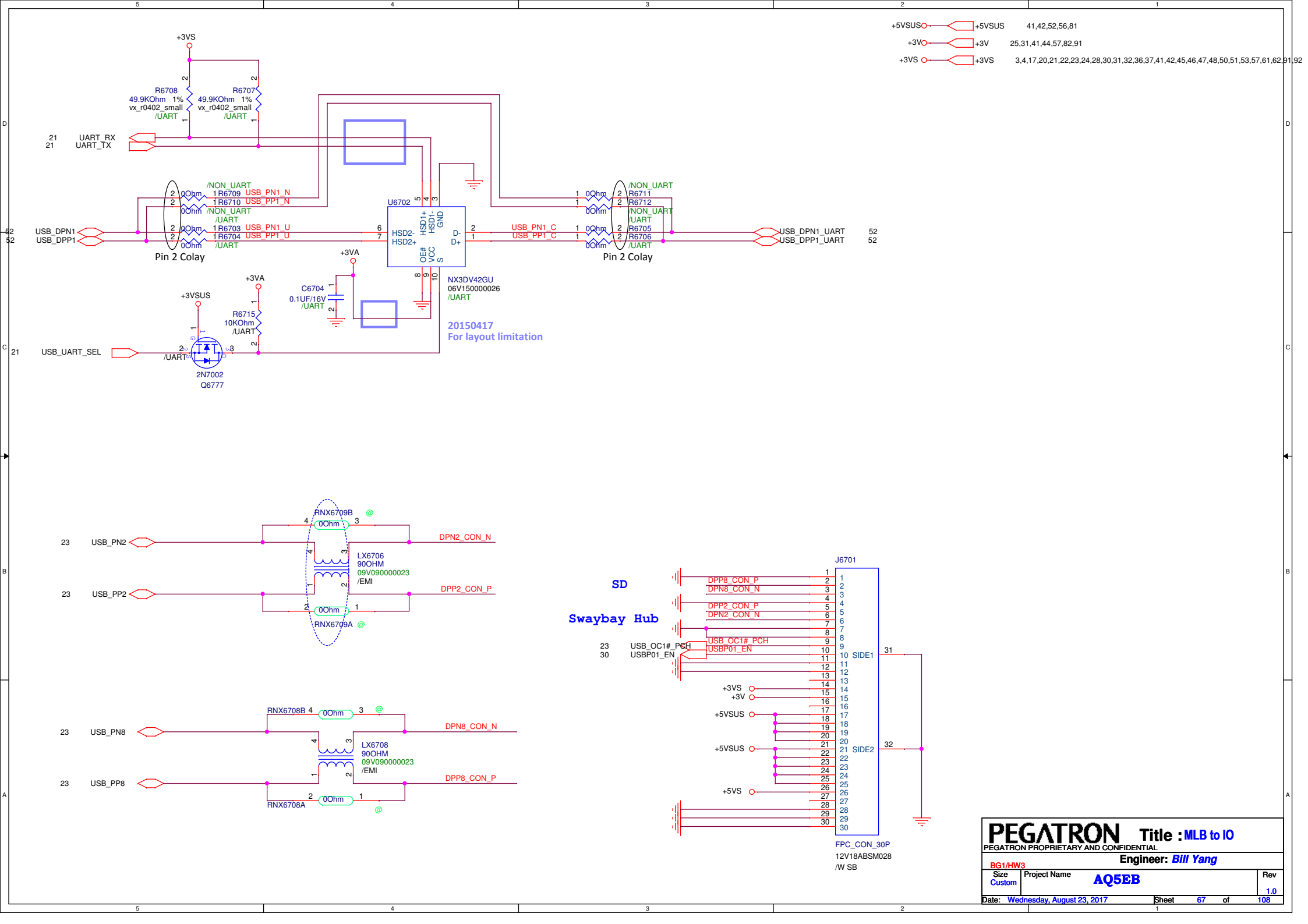




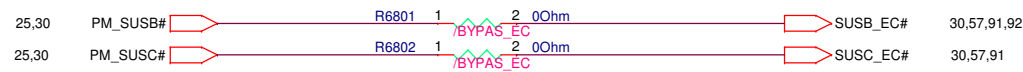
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: <b>Bill Yang</b>	
Size <b>Custom</b>	Project Name <b>AQ5EB</b>		Rev <b>1.0</b>
Date <b>Wednesday, August 23, 2017</b>		Sheet <b>65</b>	of <b>108</b>

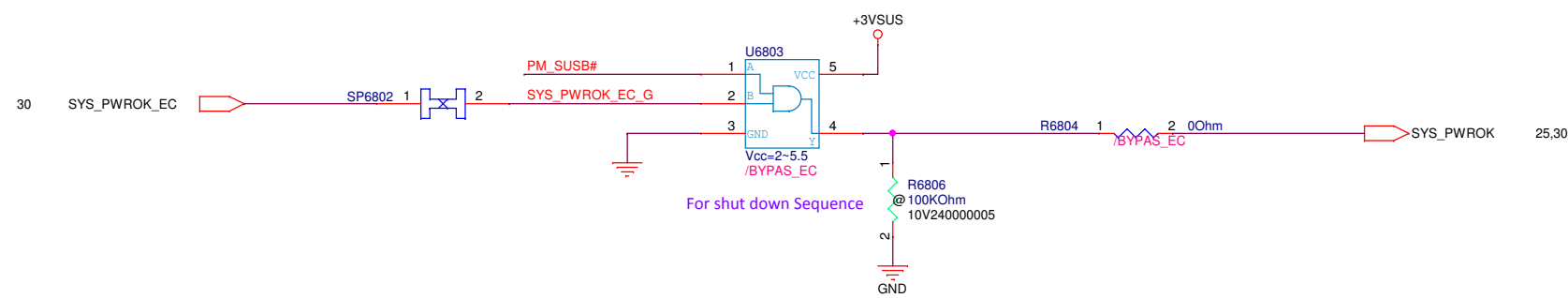
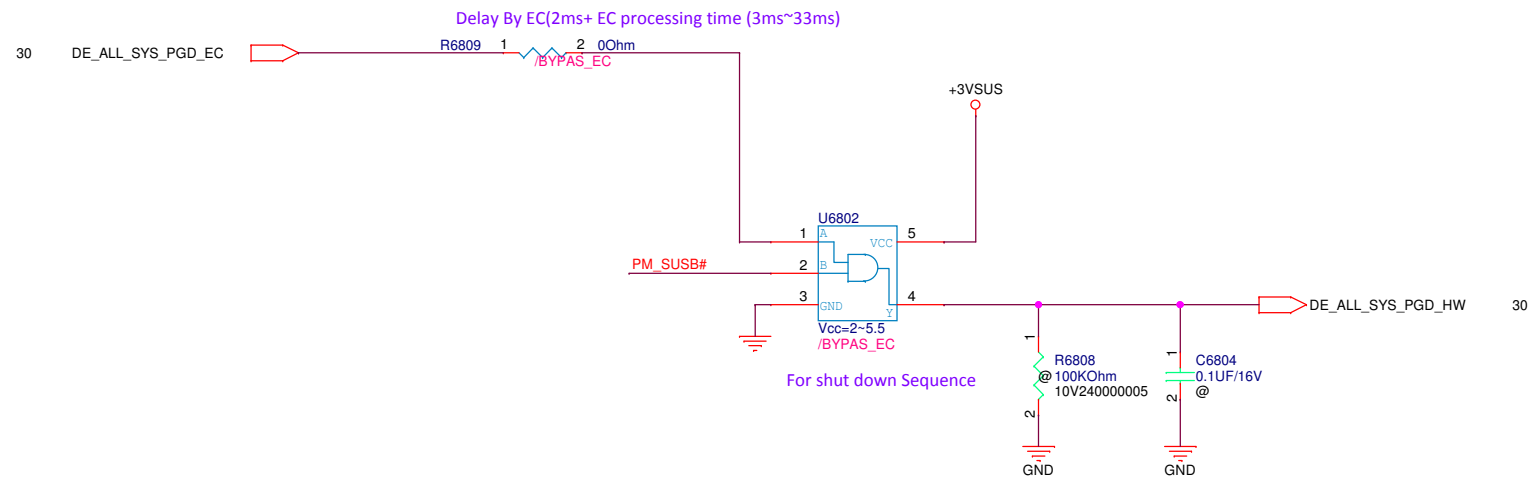




+3VSUS    +3VSUS    4,24,25,26,28,30,31,33,42,51,53,62,67,81,92  
+3VA    +3VA    24,30,31,36,43,53,56,57,67,81,88,93



For Intel power sequence request  
ALL\_SYS\_PWRGD to Delay\_ALL\_SYS\_PGD >2ms





D

D

C

C

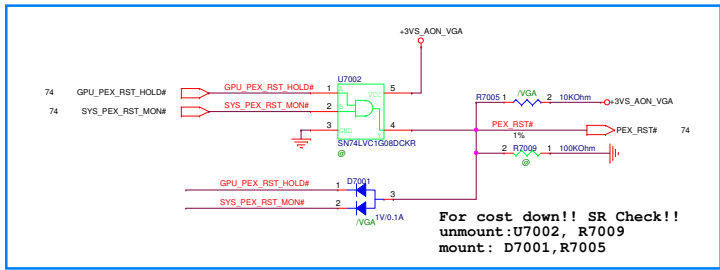
B

B

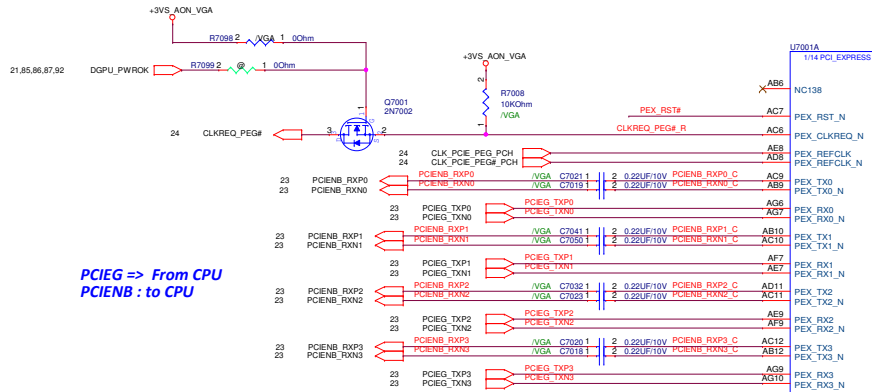
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A

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Size A	Document Number <Doc>		Rev <RevCode>
Date:	Wednesday, August 23, 2017		Sheet 69 of 108

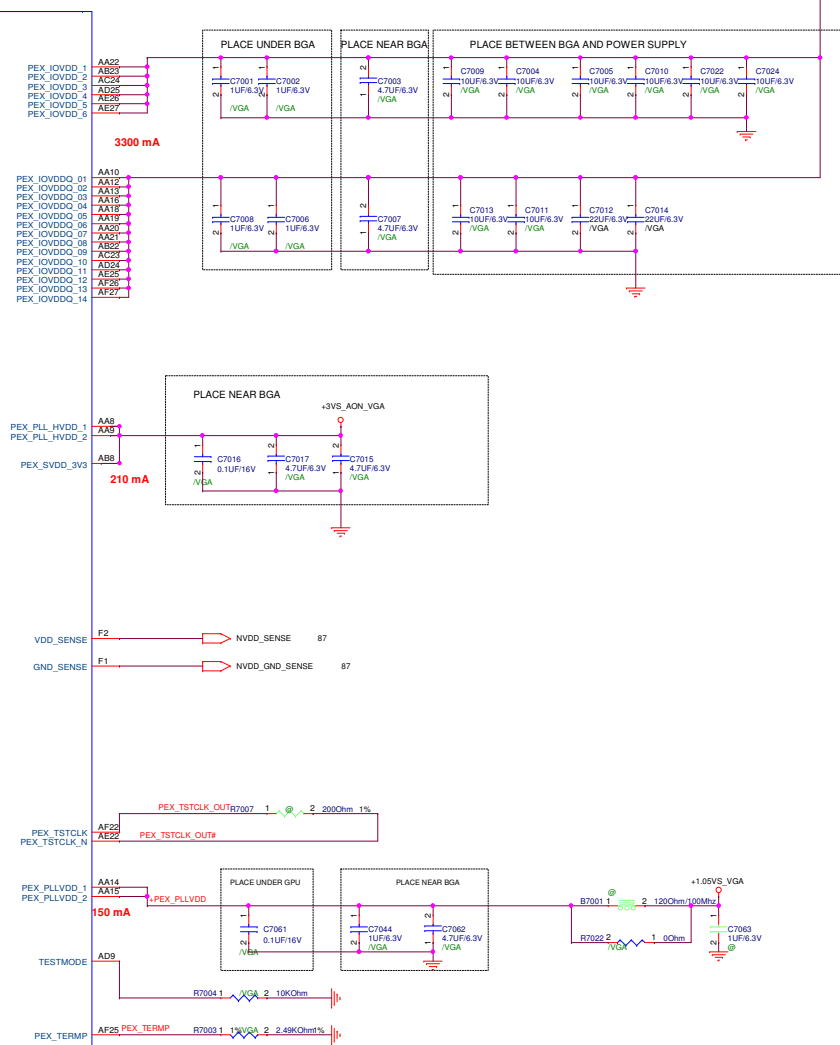


+3VS\_AON\_VGA 57.72,74,75,91  
+1.05VS\_VGA 57,71,72,86

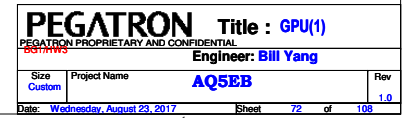


PCIe => From CPU  
PCIENB : to CPU

PCI Express decoupling capacitors  
support gen2 ==> 0.1uF  
support gen3 ==> 0.22uF

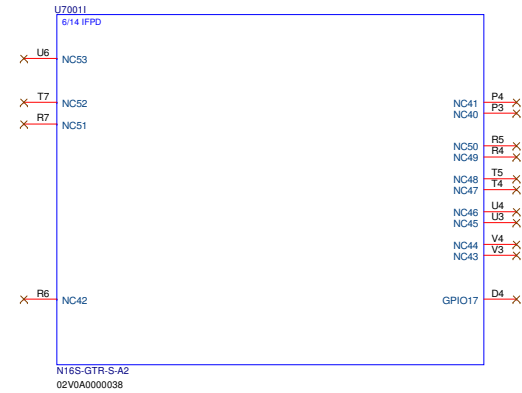
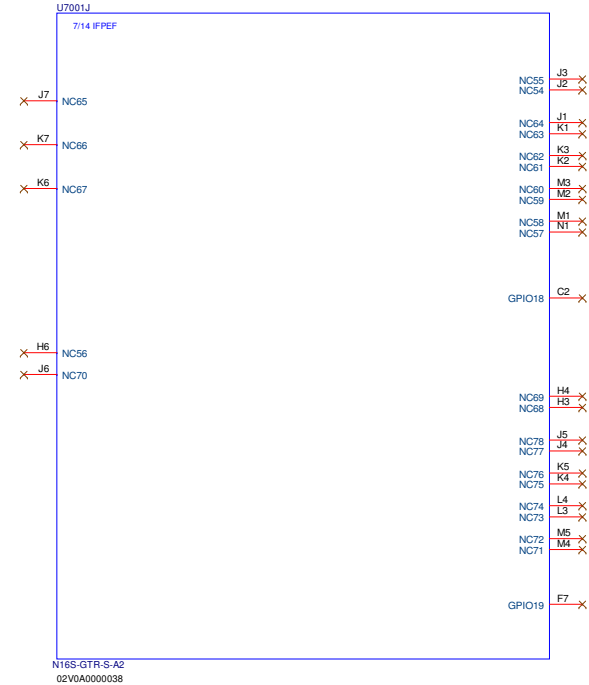
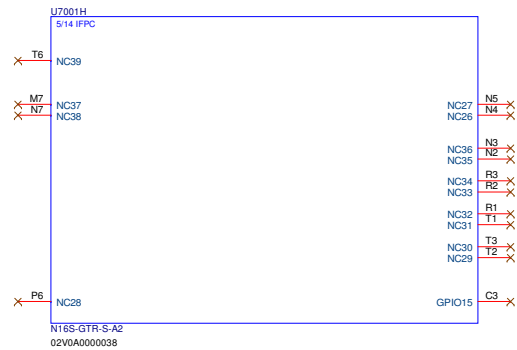
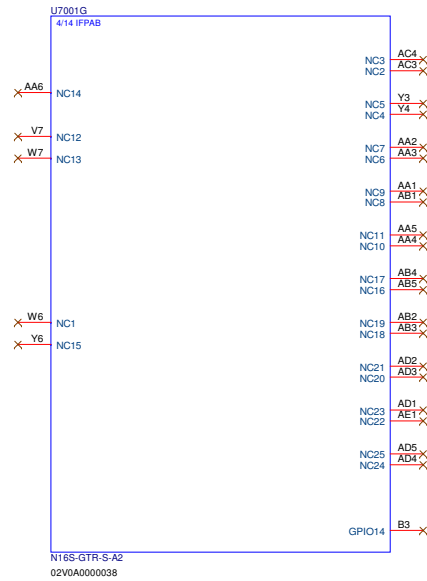


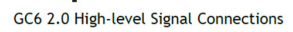
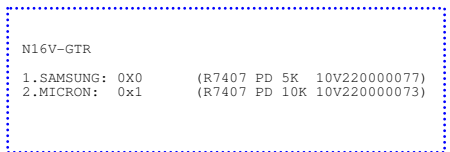
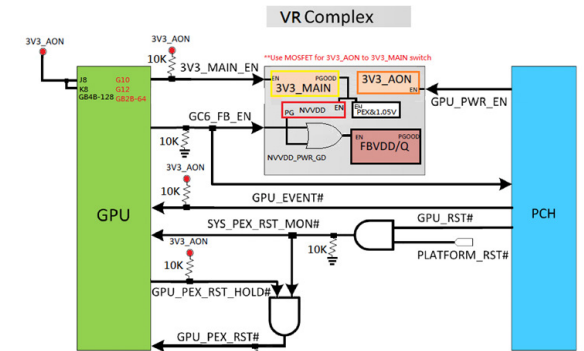






# LVDS



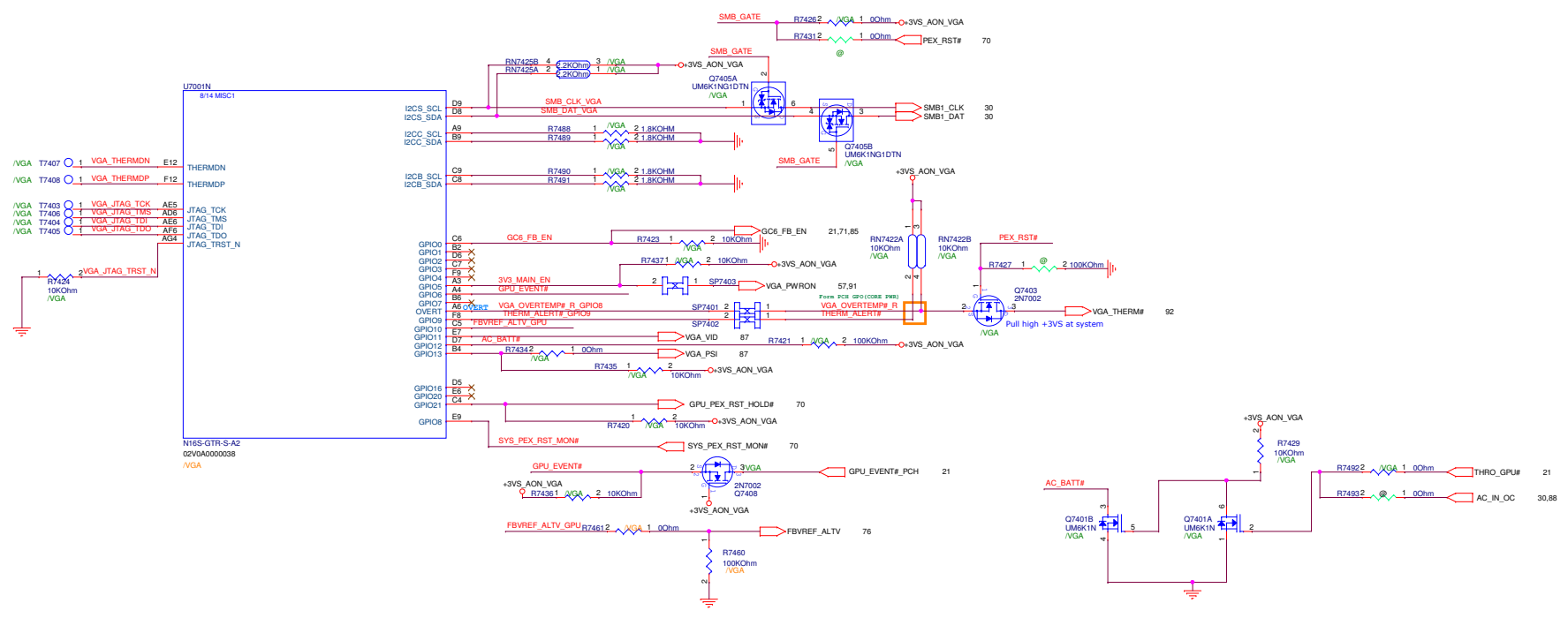


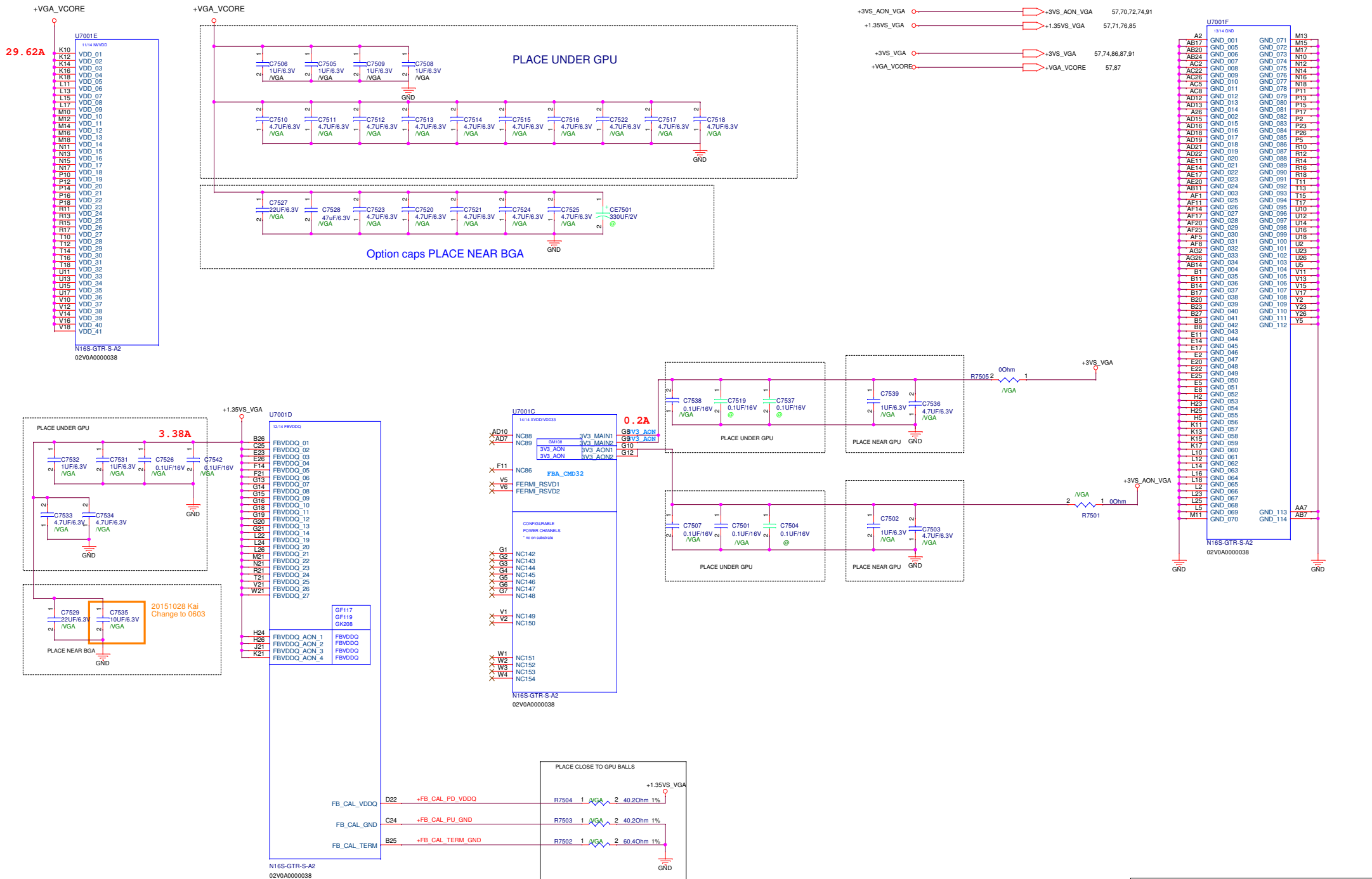
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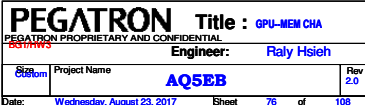
N16V-GTR
1.SAMSUNG: 0X0      (R7407 PD 5K 10V2200000077)
2.MICRON: 0x1       (R7407 PD 10K 10V2200000073)

```

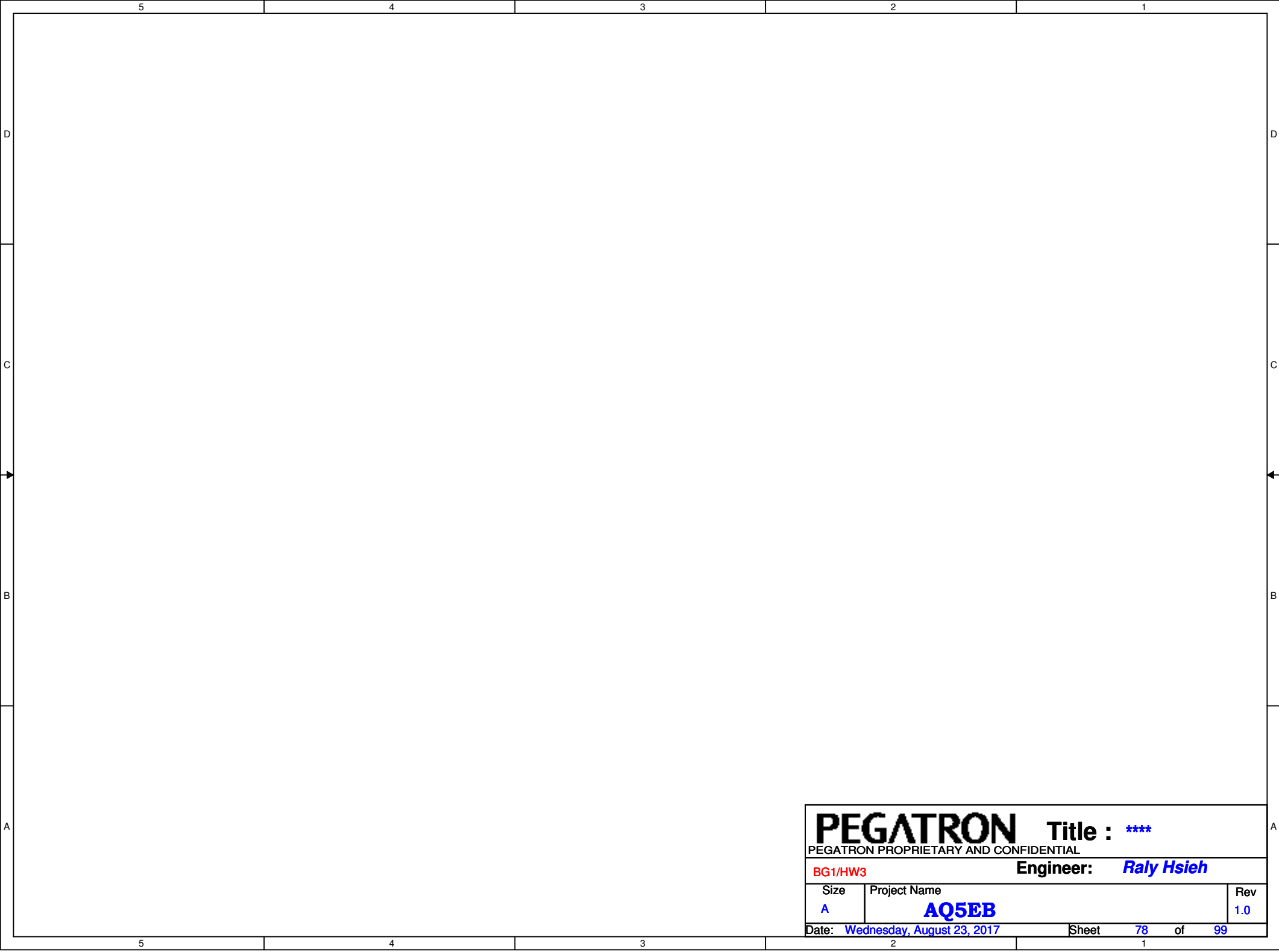
ROM_SI		ROM_SO		ROM_SCLK	
R7404	R7407	R7405	R7408	R7406	R7409
20k	N	4.99K	N	4.99K	N
N	45.3k	4.99K	N	4.99K	N
34.8k	N	4.99K	N	4.99K	N
N	30.1k	4.99K	N	4.99K	N
10k	N	N	4.99K	N	4.99K
20k	N	N	4.99K	N	4.99K
N	20k	N	4.99K	N	4.99K
N	30.1k	N	4.99K	N	4.99K











PEGATRON

Title : \*\*\*\*

PEGATRON PROPRIETARY AND CONFIDENTIAL

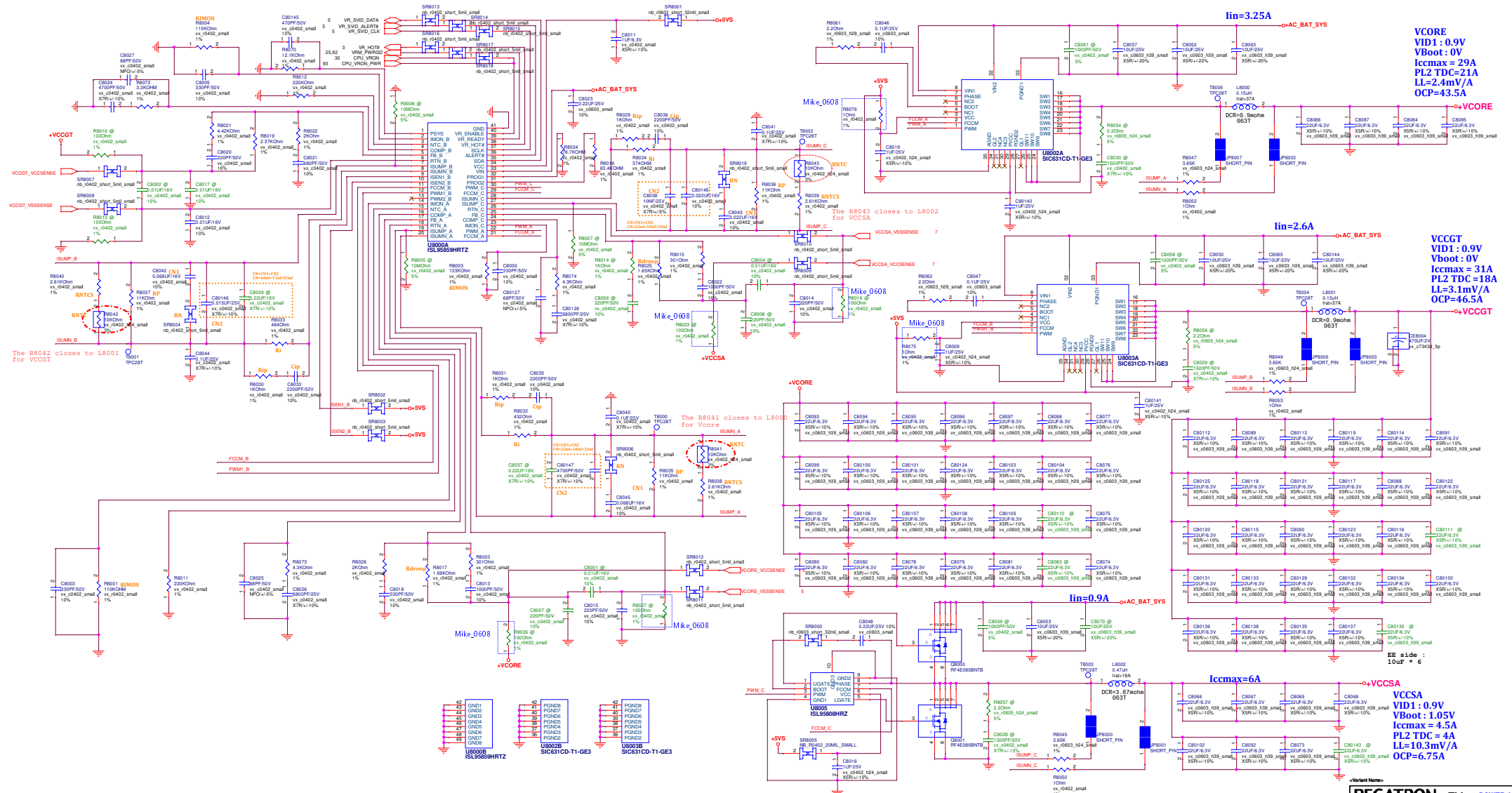
BG1/HW3

Engineer: Raly Hsieh

Size A	Project Name AQ5EB	Rev 1.0
Date: Wednesday, August 23, 2017	Sheet 78 of 99	

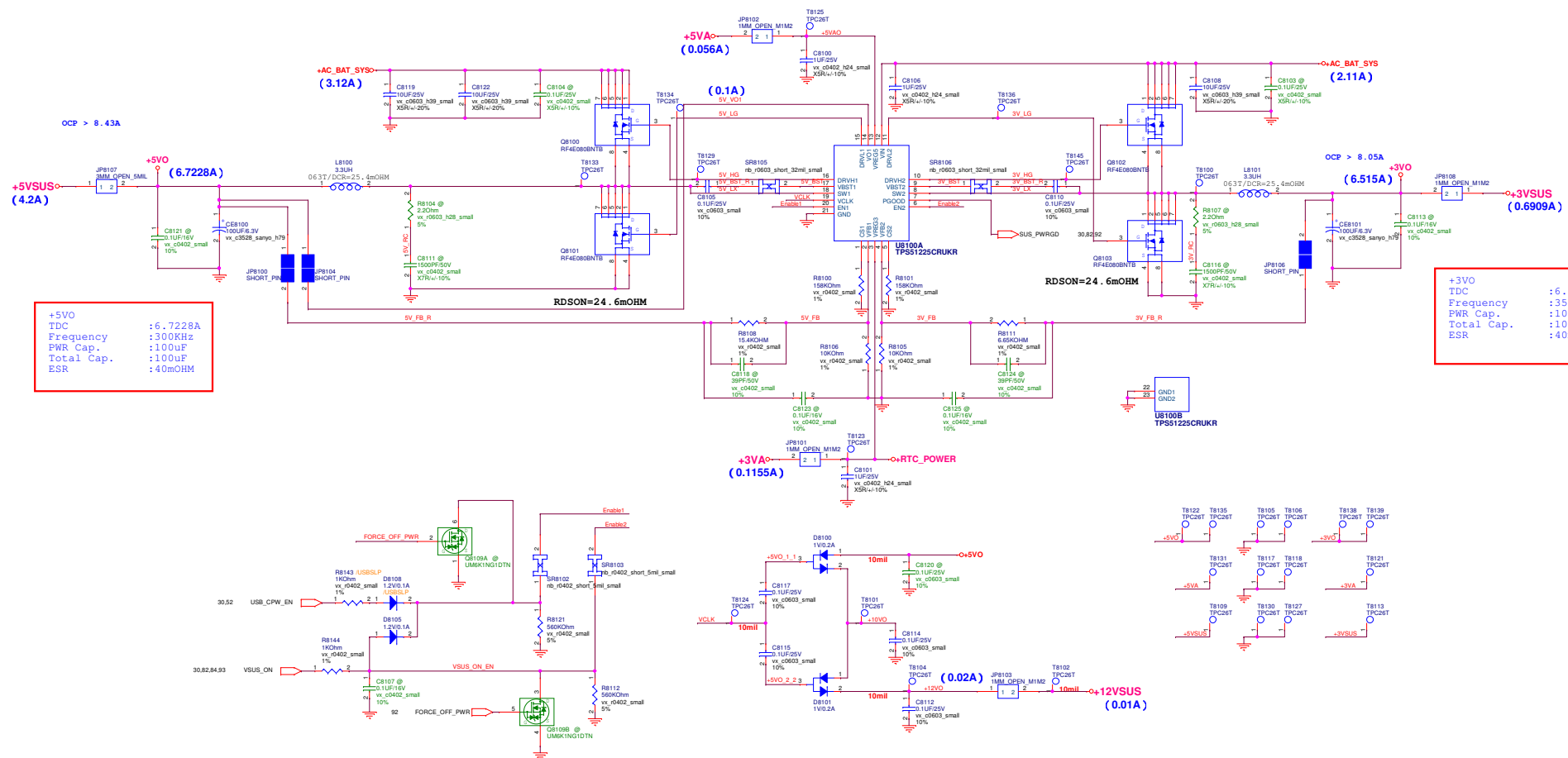
5					4					3					2					1																																																																																																																																																									
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## VCORE & VCCGT & VCCSA POWER SUPPLY

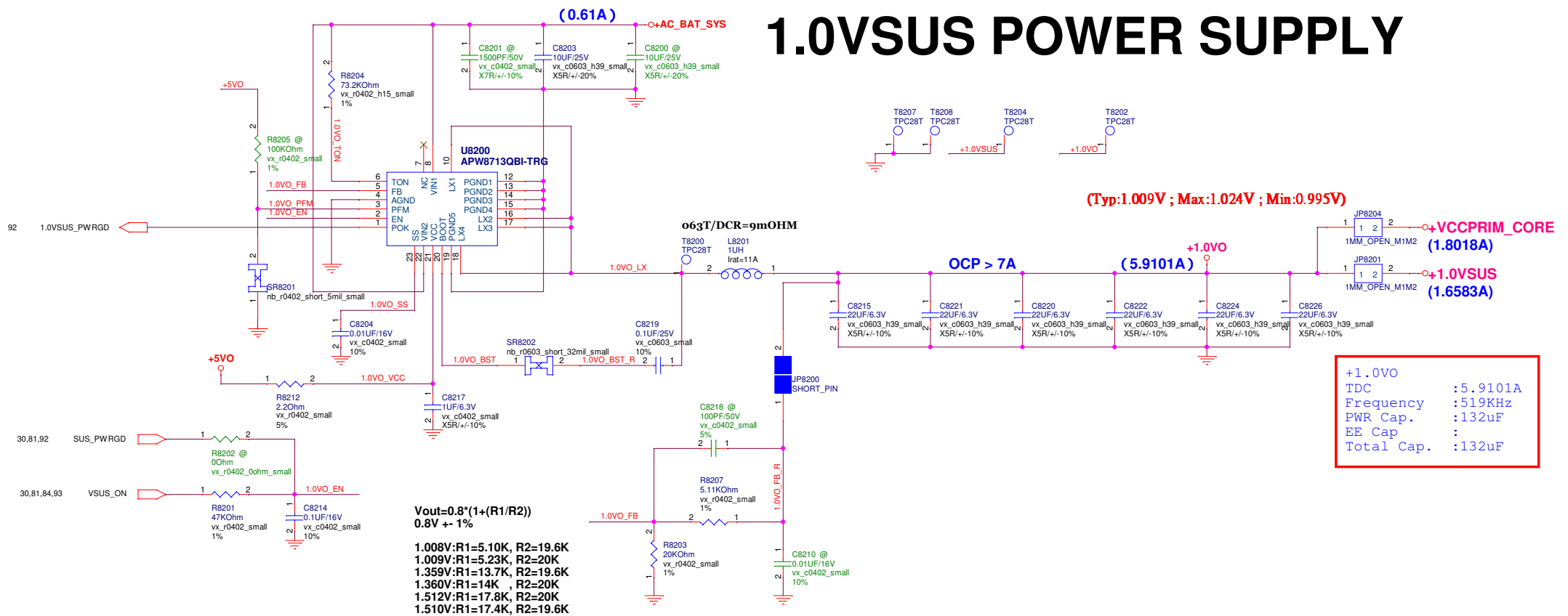




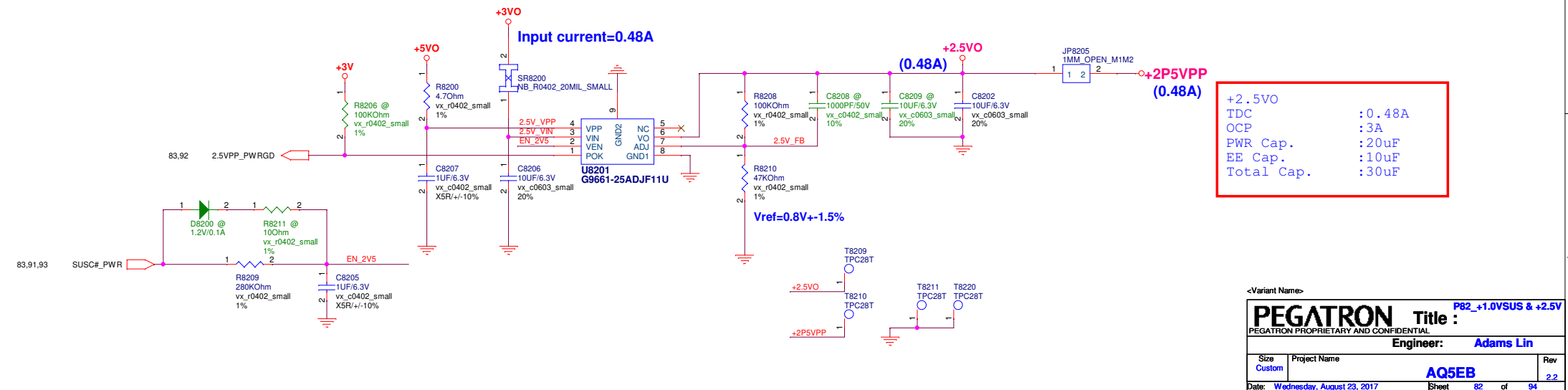
## 5VO & 3VO POWER SUPPLY



## 1.0VSUS POWER SUPPLY



## 2.5V POWER SUPPLY



# DDR & VTT POWER SUPPLY

**VID Reference Voltage (V)**

VID	Reference Voltage (V)
High	0.675
Low	0.75

**SKU Load current (A) Low-side MOSFET (pcs) Output 22uF/6.3V MLCC (pcs)**

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

**PEGATRON** Title : POWER\_DDR & VTT  
PEGATRON PROPRIETARY AND CONFIDENTIAL  
BG1-POWER Engineer: Adams Lin  
Size Project Name  
Custom A05EB  
Date: Wednesday, August 23, 2017 Sheet 83 of 94

# DDR & VTT POWER SUPPLY

VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

**PEGATRON** Title : POWER\_DDR & VTT

PEGATRON PROPRIETARY AND CONFIDENTIAL

Size Custom Project Name AQ5EB Rev 2.2

Date: Wednesday, August 23, 2017 Sheet 83 of 94

# DDR & VTT POWER SUPPLY

VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

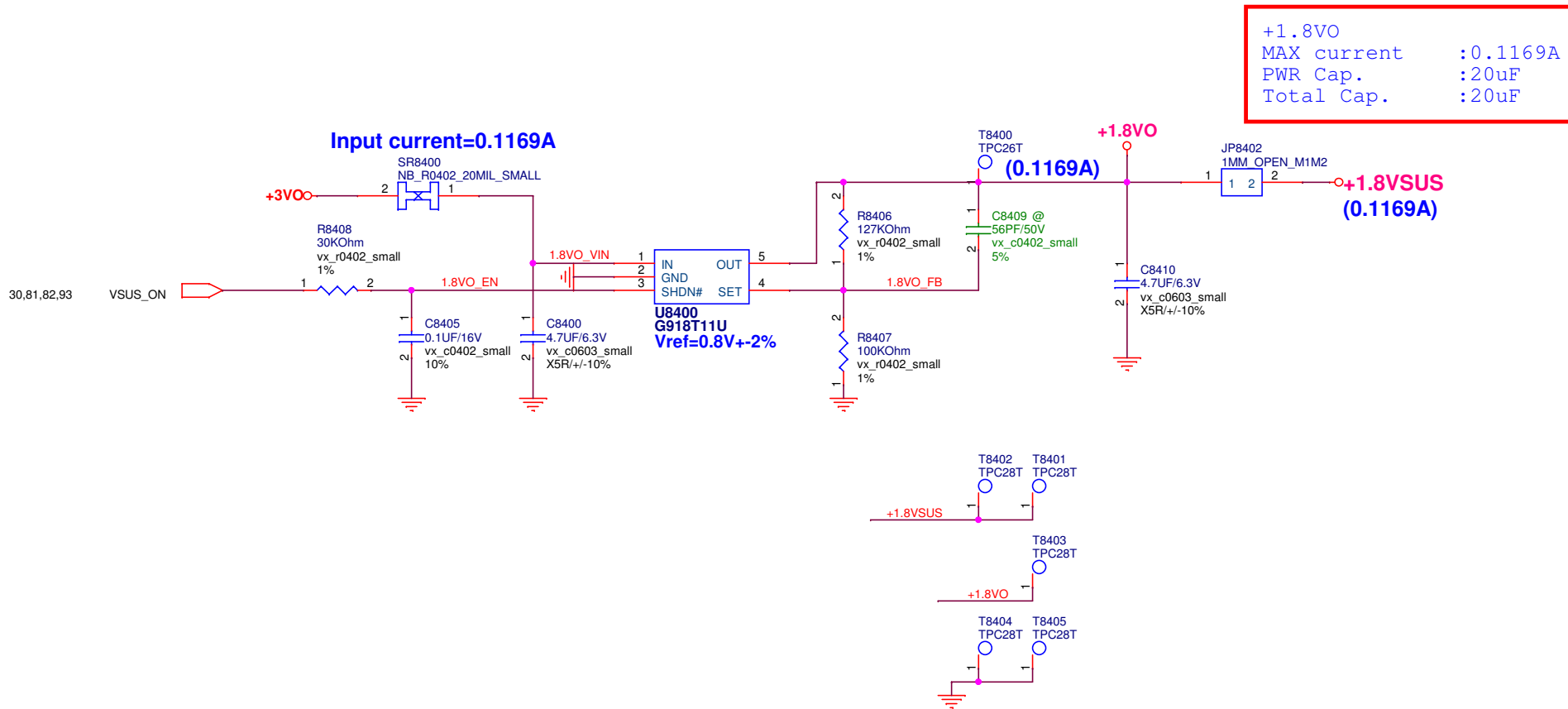
**PEGATRON** Title : POWER\_DDR & VTT

PEGATRON PROPRIETARY AND CONFIDENTIAL

Size Custom Project Name AQ5EB Rev 2.2

Date: Wednesday, August 23, 2017 Sheet 83 of 94

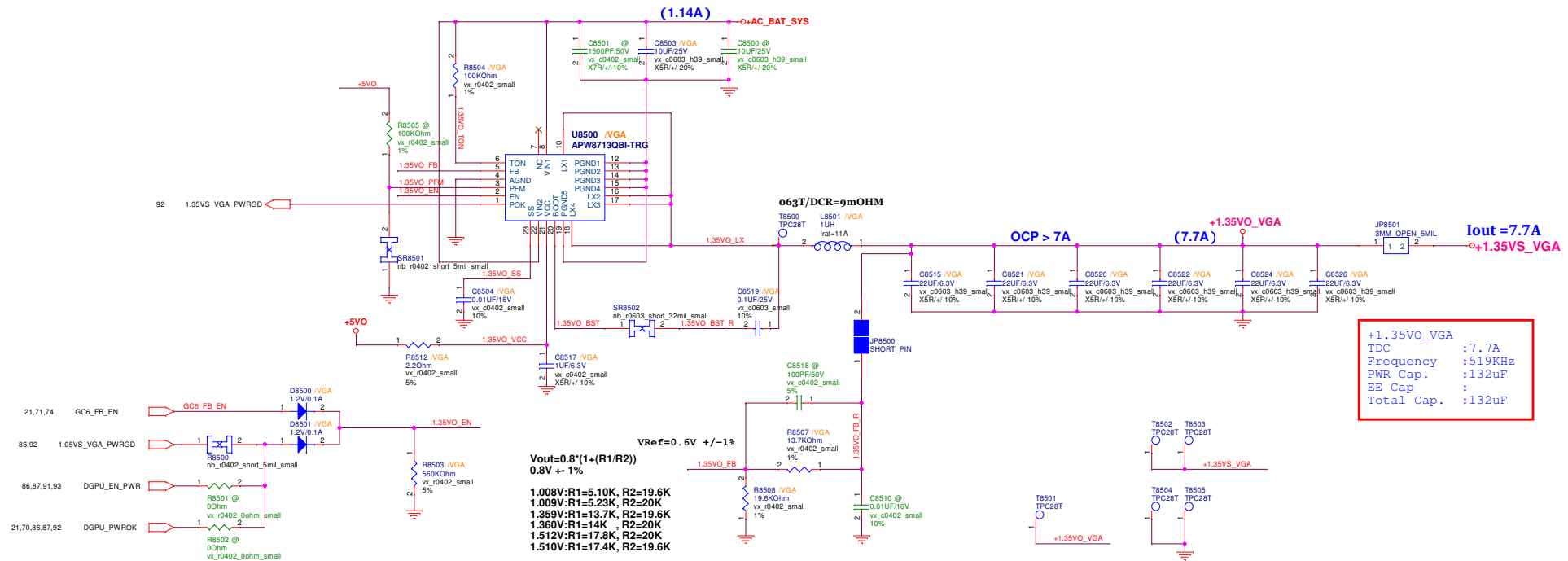
# 1.8VSUS POWER SUPPLY



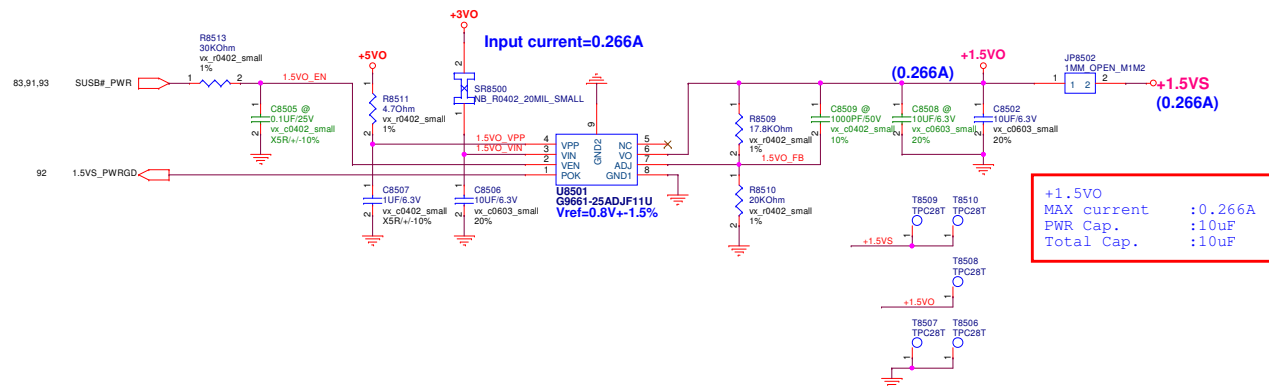
<Variant Name>

<b>PEGATRON</b>		<b>Title : POWER_+1.8VSUS</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>Engineer:</b>		<b>Adams Lin</b>	
Size Custom	Project Name <b>AQ5EB</b>		Rev 2.2
Date: <b>Wednesday, August 23, 2017</b>		Sheet <b>84</b> of <b>94</b>	

# 1.35VS\_VGA POWER SUPPLY



## 1.5VS POWER SUPPLY



<Variant Name>

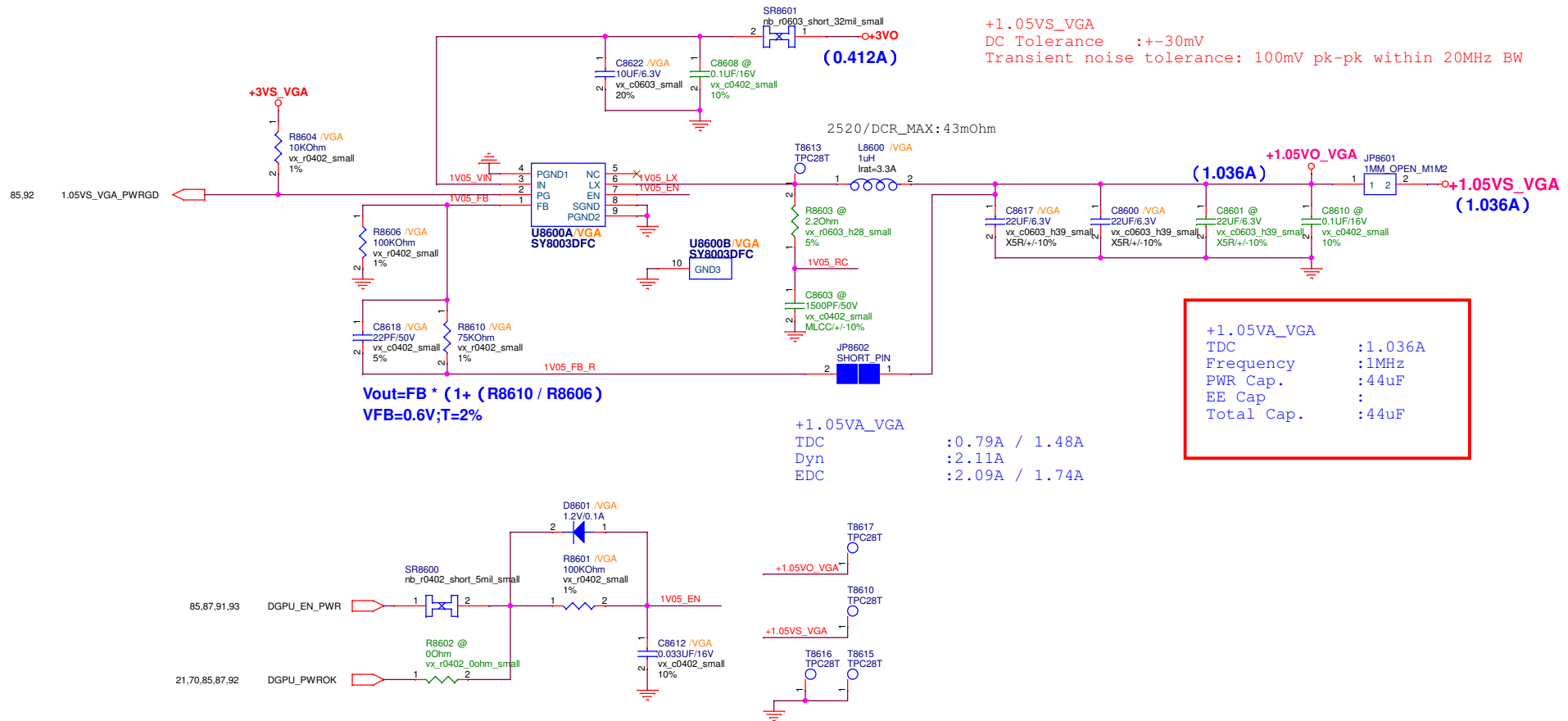
**PEGATRON** Title: **POWER\_+1.5VS**  
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: **Adams Lin**

Size: Custom Project Name: **AQ5EB** Rev: **22**

Date: Wednesday, August 23, 2017 Sheet: 85 of 94

# 1.05VS\_VGA POWER SUPPLY



<Variant Name>

<b>PEGATRON</b>		<b>Title : +1.05VS_VGA</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		<b>Engineer: Adams Lin</b>	
<b>Size</b> Custom	<b>Project Name</b>  <b>AQ5EB</b>		<b>Rev</b> 2.2
<b>Date:</b>	<u>Wednesday, August 23, 2017</u>	<b>Sheet</b>	<u>86</u> of <u>94</u>

# VGA\_CORE POWER SUPPLY

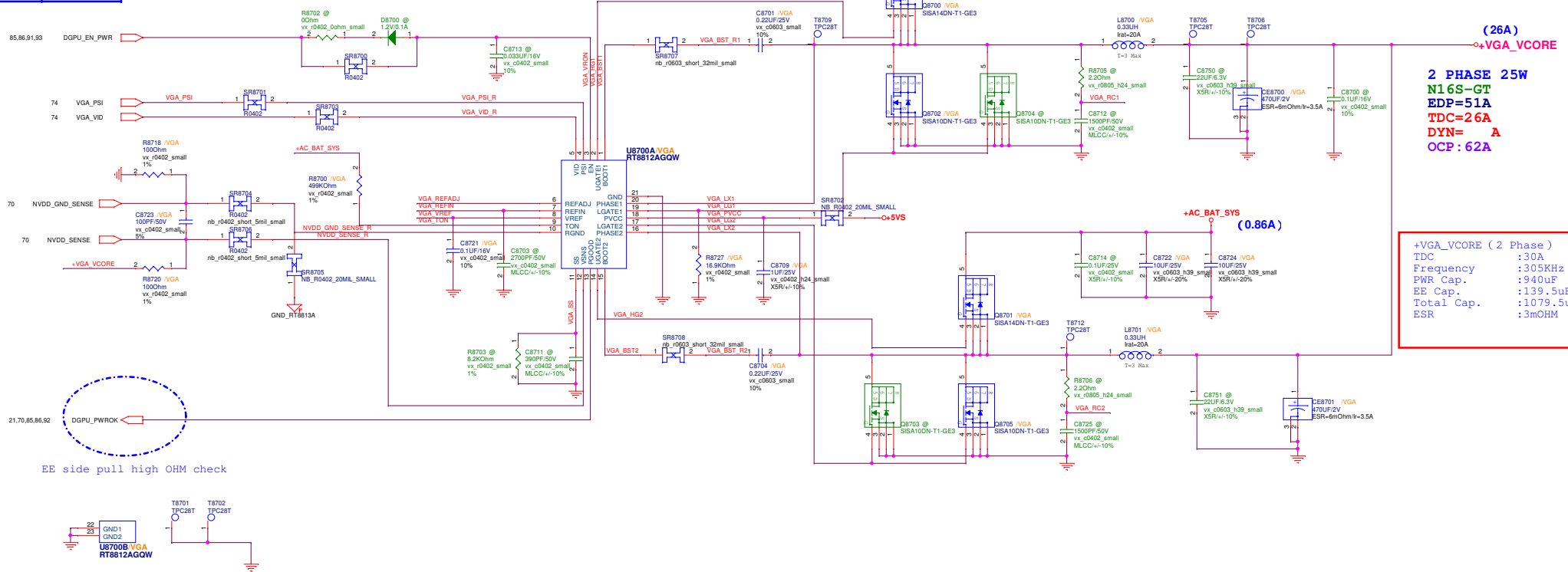
+VGA\_VCORE(Package type:N16VS-GT)  
DC Tolerance :+-20mV

Overshoot/undershoot  
Transient noise tolerance: -10% ~ +20% within 20MHz BW  
High frequency noise: 400mV pk-pk within 1GHz BW

VID:0.6V ~ 1.2V  
Number of programmable Volt: 96 levels  
Programmable volt steps: 6.25mV  
Settling Time: < 100us for rising, no restriction on falling

	N16	N16S_GT
R8723	39K	20K
R8721	39K	20K
R8716	1.5K	2K
R8713	31.5K	18K
C8720	>1.8nF	2.7nF
Vstep	6.25mV	6.25mV
Vmin	0.65V	0.6V
Vmax	1.15V	1.2V
Vboot	0.875V	0.9V
openVR Config	A	B

VGA_PSI#	VO_action
~ 0.8V	1 Phase DEM
1.2 ~ 1.8V	1 Phase FCCM
2.4V ~	2 Phase FCCM



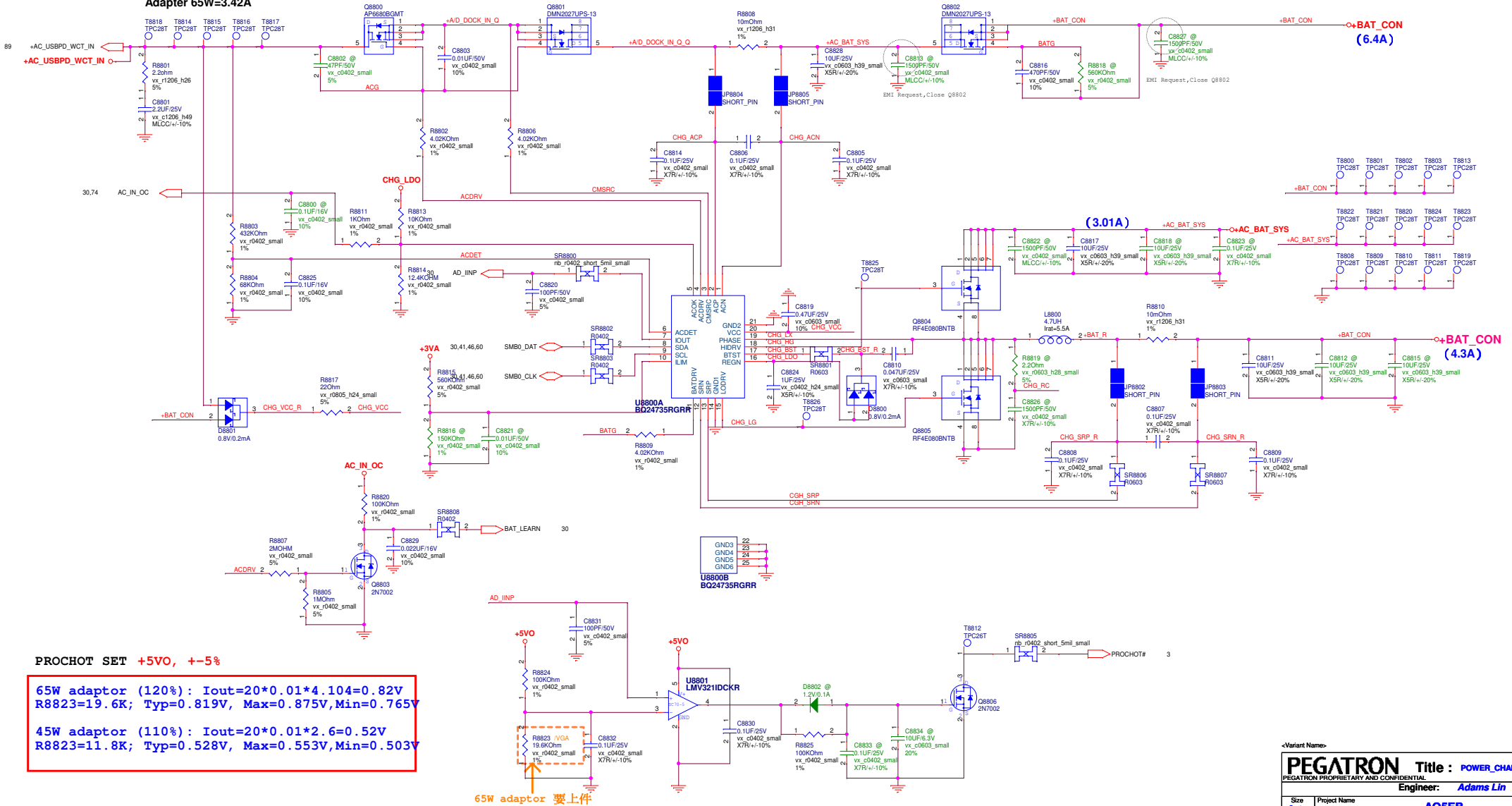
**2 PHASE 25W**  
**N16S-GT**  
**EDP=51A**  
**TDC=26A**  
**DYN= A**  
**OCF: 62A**

+VGA\_VCORE (2 Phase)  
TDC :30A  
Frequency :305KHz  
PNR Cap. :940uF  
EE Cap. :139.5uF  
Total Cap. :1079.5uF  
ESR :3mOHM

EE side pull high OHM check

# BATTERY CHARGER

Adapter 45W=2.37A  
Adapter 65W=3.42A



PROCHOT SET +5VO, +-5%

65W adaptor (120%):  $I_{out}=20 \times 0.01 \times 4.104 = 0.82V$   
R8823=19.6K; Typ=0.819V, Max=0.875V, Min=0.765V

45W adaptor (110%):  $I_{out}=20 \times 0.01 \times 2.6 = 0.52V$   
R8823=11.8K; Typ=0.528V, Max=0.553V, Min=0.503V

65W adaptor 要上件

<Variant Name>

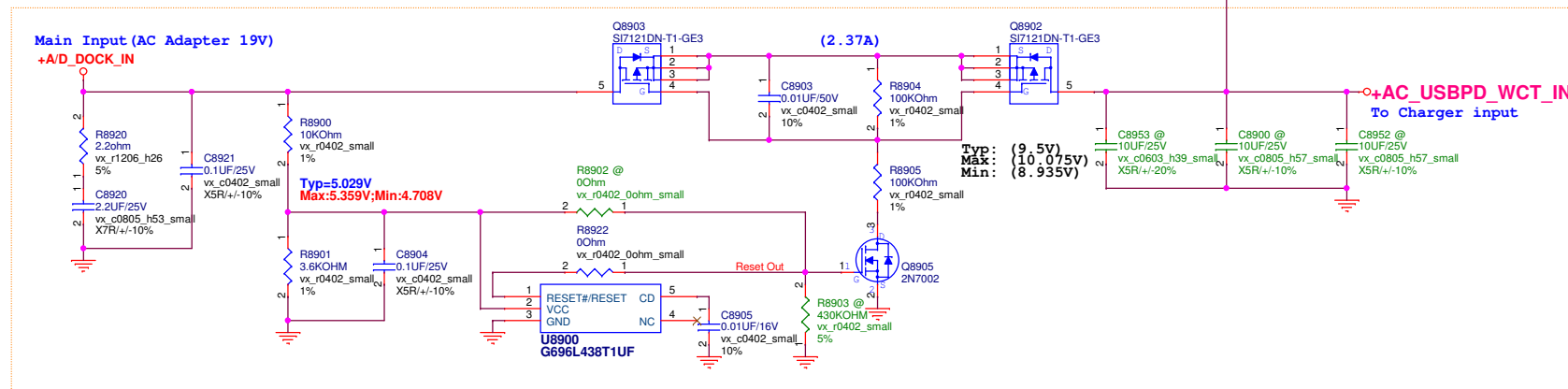
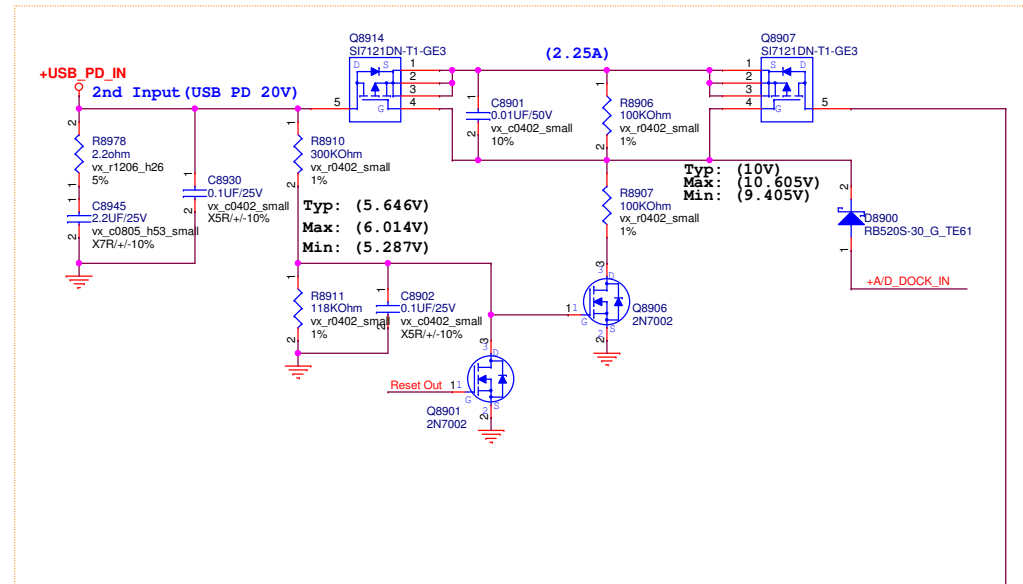
**PAGATRON** Title : POWER\_CHARGER  
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Adams Lin

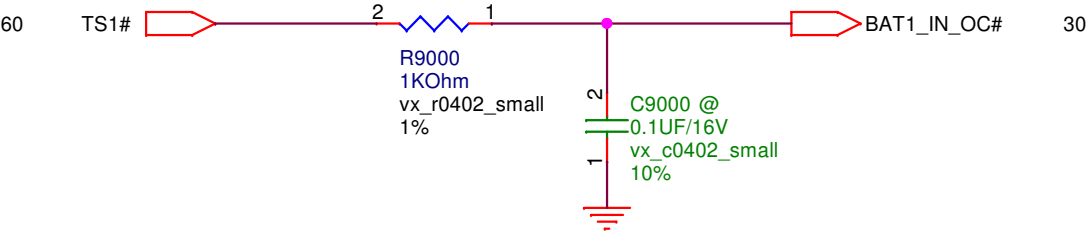
Size Custom Project Name AQ5EB Rev 2.2  
Date: Wednesday, August 23, 2017 Sheet 66 of 64



# 2 Input switch Circuit



BATTERY IN DETECT



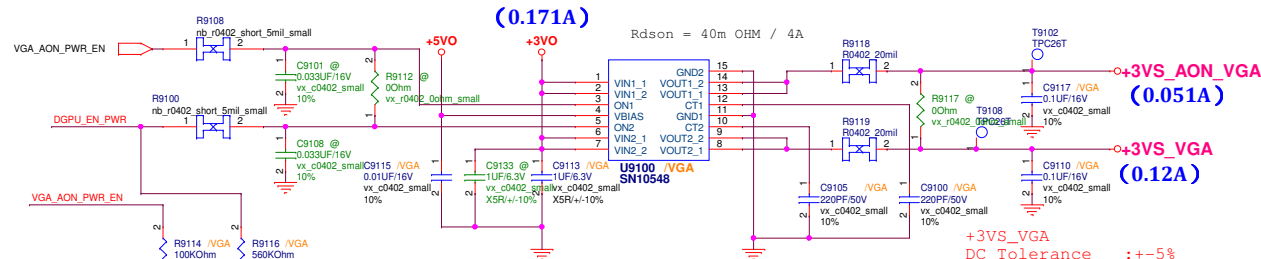
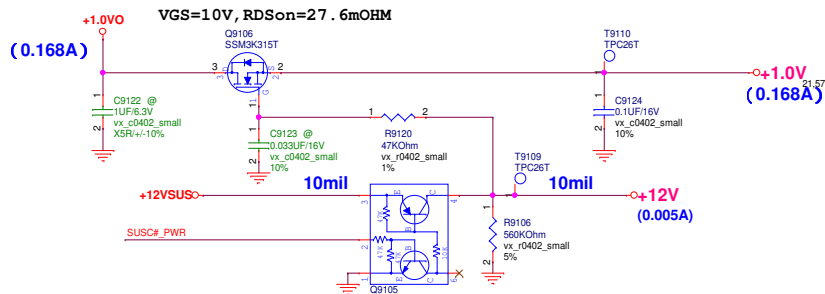
<Variant Name>

<b>PEGATRON</b>		Title : <b>POWER_DETECT</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: <b>Adams Lin</b>	
Size <b>Custom</b>	Project Name <b>AQ5EB</b>		Rev <b>2.2</b>
Date:	<b>Wednesday, August 23, 2017</b>	Sheet	<b>90</b> of <b>94</b>

# SUSC#\_PWR POWER

# SUSB#\_PWR POWER

# DSC\_VGA\_PWR POWER



GC6 Cold boot/Optimus:  
3V3\_AON & 3V3\_MAIN --> NVVDD --> PEX\_VDD --> FBVDD/Q

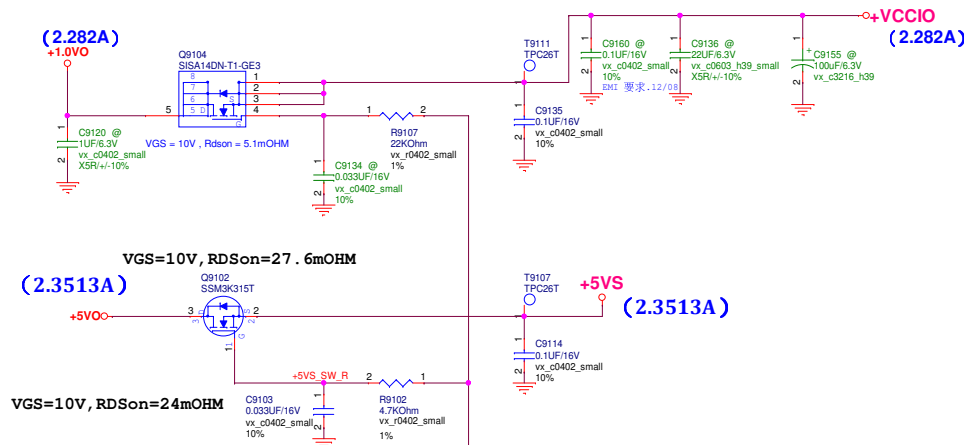
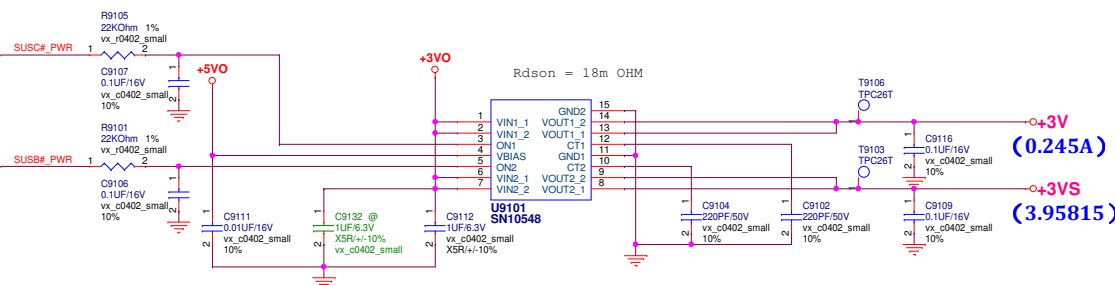
GC6 2.0 Exit:  
3V3\_MAIN --> NVVDD --> PEX\_VDD

## Power up Sequencing

- 1.The ramp time for any rail must be more 40us and is recommended to be less than 2ms
- 2.The previous power rail must ramp up to 90% before the next power rail can start ramping up

## Power down Sequencing

- 1.There is no specific power down sequence
- 2.Residual voltage from power down must not violate ther power up sequence when back to back GPU power down and power up event take place



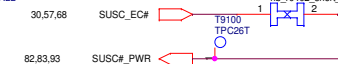
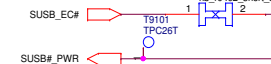
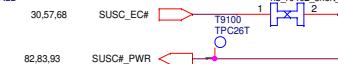
## DSC\_VGA\_PWR POWER Control

## SUSC#\_PWR POWER Control

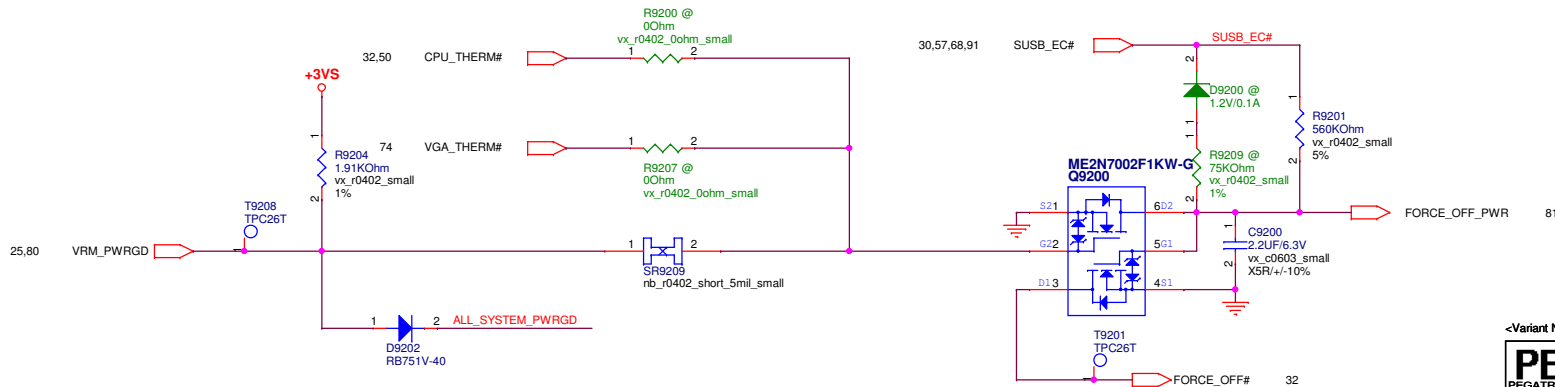
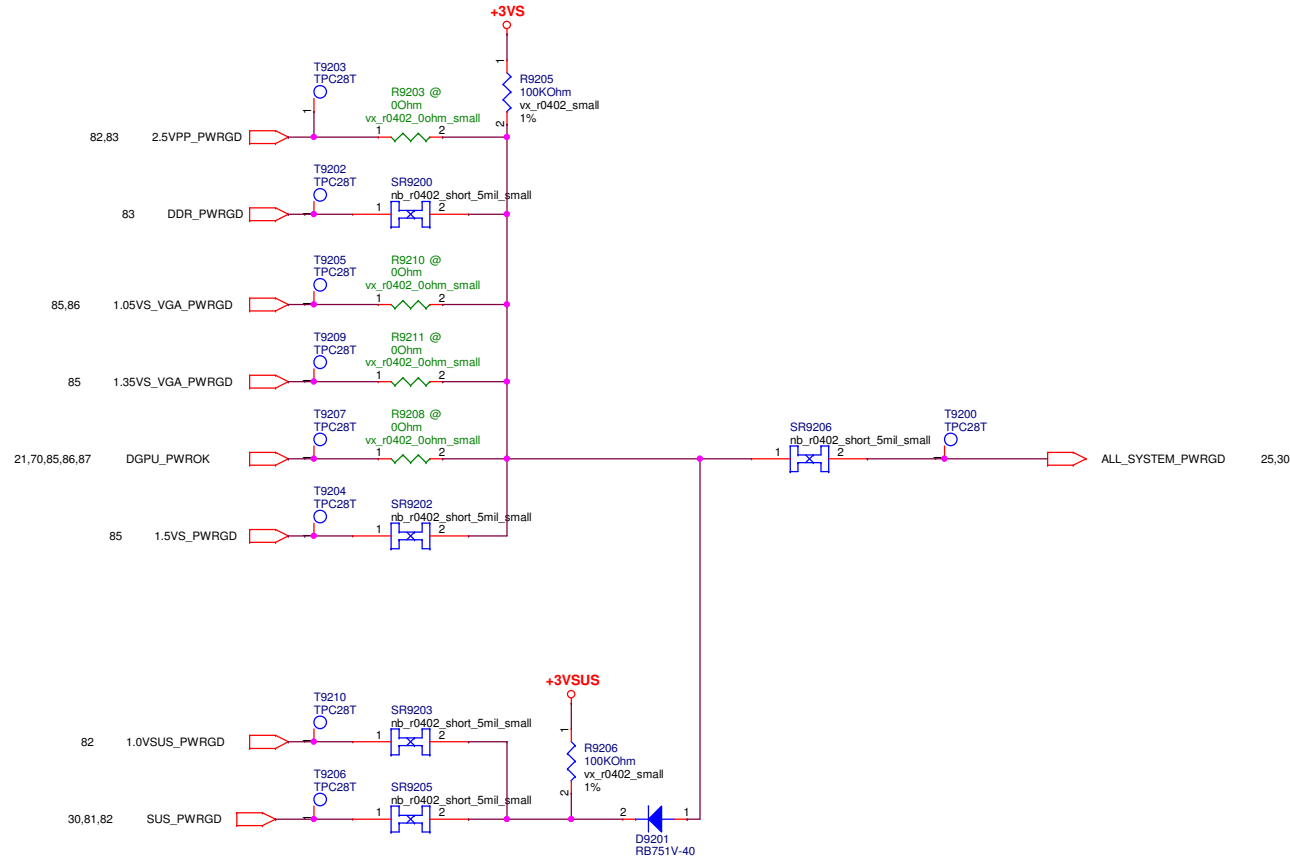
<Variant Name>

<b>PEGATRON</b>		Title : <b>POWER_LOAD SWITCH</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer:		<b>Adams Lin</b>	
Size Custom	Project Name	<b>AQ5EB</b>	Rev 2.2
Date: <b>Wednesday, August 23, 2017</b>		Sheet <b>91</b> of <b>94</b>	

## SUSB#\_PWR POWER Control



# POWER GOOD DETECTOR

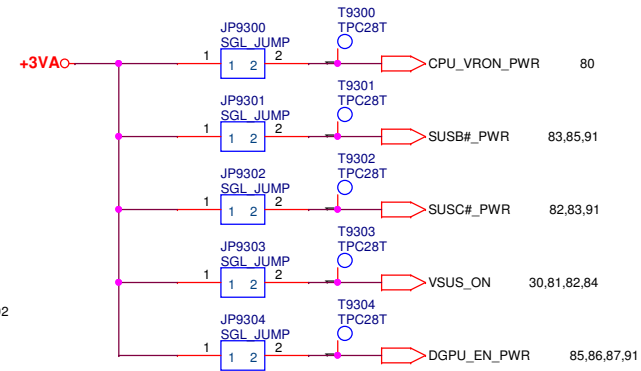


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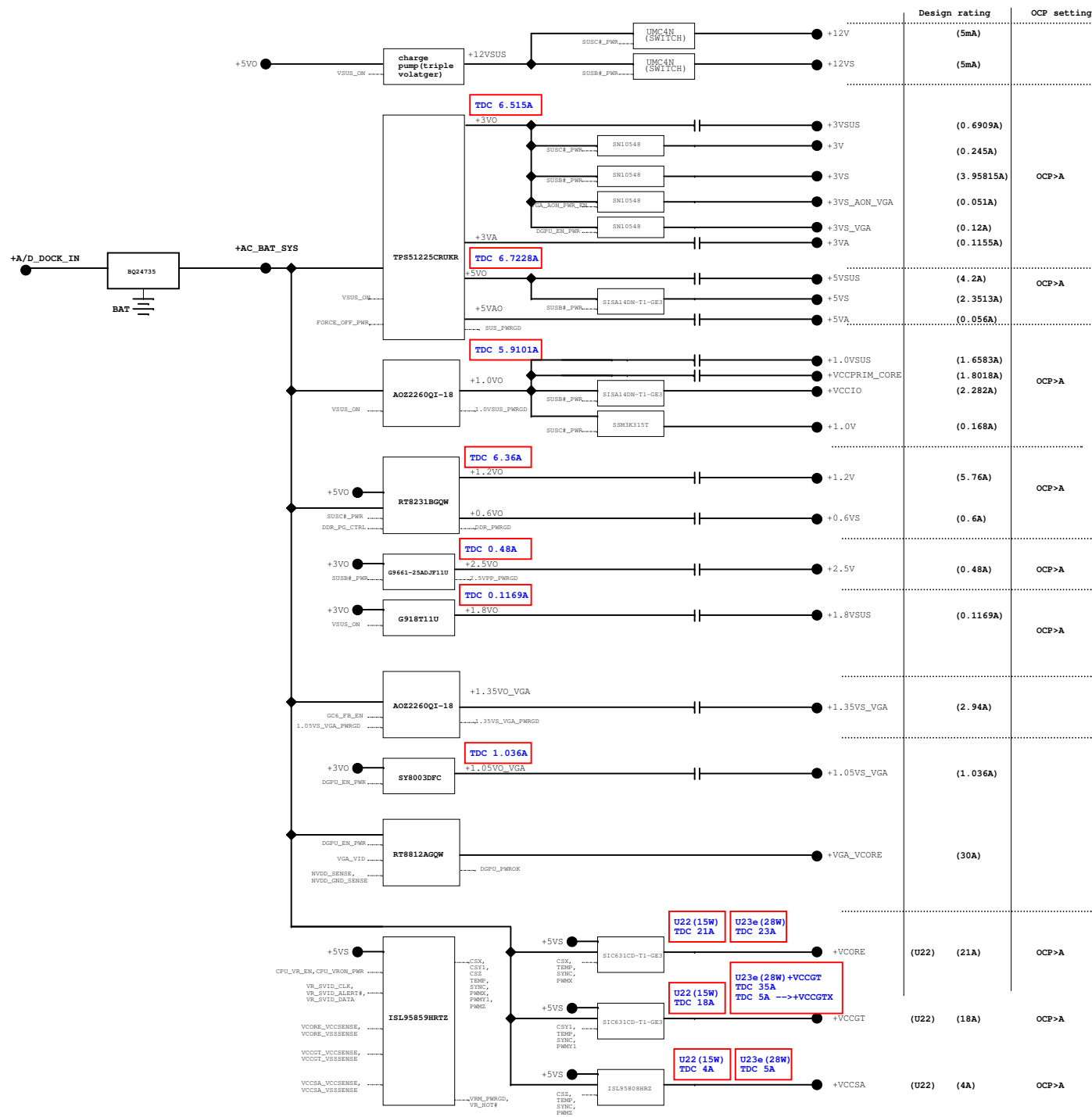
<b>PEGATRON</b>		Title : <b>POWER_PROTECT</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer: <b>Adams Lin</b>			
Size Custom	Project Name	<b>AQ5EB</b>	Rev 2.2
Date:	<b>Wednesday, August 23, 2017</b>	Sheet	<b>92 of 94</b>

+USB_PD_IN	→	+USB_PD_IN	42,89
+A/D_DOCK_IN	→	+A/D_DOCK_IN	60,89
+AC_USBDPD_WCT_IN	→	+AC_USBDPD_WCT_IN	88,89
+AC_BAT_SYS	→	+AC_BAT_SYS	41,43,45,80,81,82,83,85,87,88
+BAT_CON	→	+BAT_CON	60,88
+RTC_POWER	→	+RTC_POWER	81
+5VA	→	+5VA	31,56,81
+3VA	→	+3VA	24,30,31,36,43,53,56,57,67,81,88
+5VO	→	+5VO	26,81,82,83,85,88,91
+3VO	→	+3VO	81,82,84,85,86,91
+2.5VO	→	+2.5VO	82
+1.8VO	→	+1.8VO	84
+1.5VO	→	+1.5VO	85
+1.2VO	→	+1.2VO	83
+1.05VO_VGA	→	+1.05VO_VGA	86
+1.0VO	→	+1.0VO	82,91
+0.6VO	→	+0.6VO	83
+12VSUS	→	+12VSUS	81,91
+5VSUS	→	+5VSUS	41,42,52,56,67,81
+3VSUS	→	+3VSUS	4,24,25,26,28,30,31,33,42,51,53,62,67,68,81,92
+1.8VSUS	→	+1.8VSUS	9,21,24,26,84
+1.0VSUS	→	+1.0VSUS	26,82
+12V	→	+12V	91
+2P5VPP	→	+2P5VPP	16,17,57,82
+1.2V	→	+1.2V	4,7,15,16,17,18,57,83
+1.0V	→	+1.0V	7,57,91
+12VS	→	+12VS	28,31,57,62,91
+5VS	→	+5VS	31,36,45,46,48,50,51,56,57,67,80,87,91
+3VS	→	+3VS	3,4,17,20,21,22,23,24,28,30,31,32,36,37,41,42,45,46,47,48,50,51,53,57,61,62,67,91,92
+1.5VS	→	+1.5VS	36,57,85
+1.05VS_VGA	→	+1.05VS_VGA	57,70,71,72,86
+0.6VS	→	+0.6VS	15,17,57,83
+VCORE	→	+VCORE	5,57,80
+VCCGT	→	+VCCGT	6,57,80
+VCCSA	→	+VCCSA	7,57,80
+VCCIO	→	+VCCIO	3,7,57,91
+VCCPRIM_CORE	→	+VCCPRIM_CORE	26,82
+VGA_VCORE	→	+VGA_VCORE	57,75,87

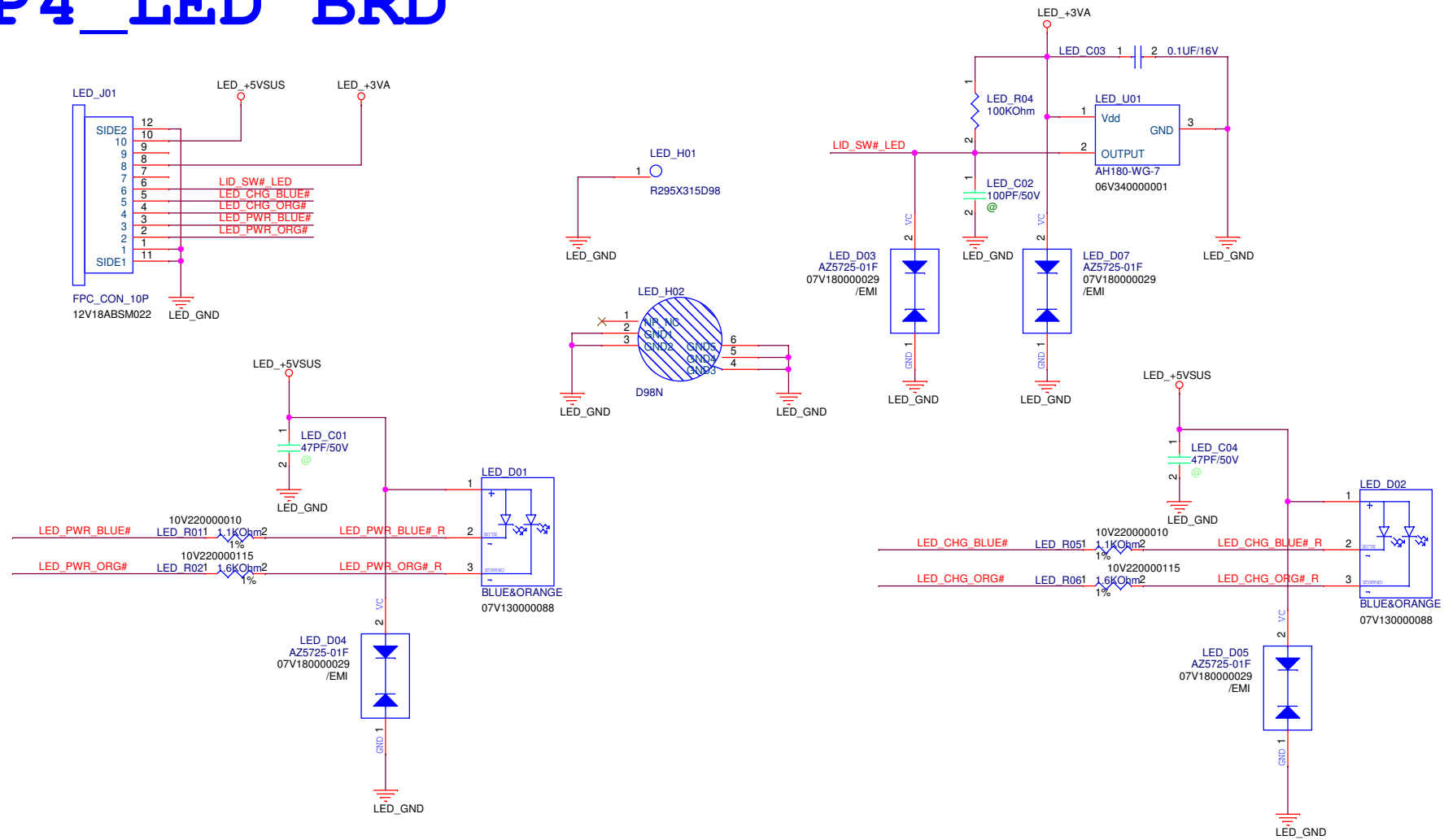
## FOR POWER TEST



<b>PEGATRON</b>		<b>Title : POWER_SIGNAL</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1-POWER</b>		<b>Engineer: Adams Lin</b>	
Size <b>B</b>	Project Name <b>AQ5EB</b>		Rev <b>2.2</b>
Date: <b>Wednesday, August 23, 2017</b>		Sheet <b>93</b>	of <b>94</b>

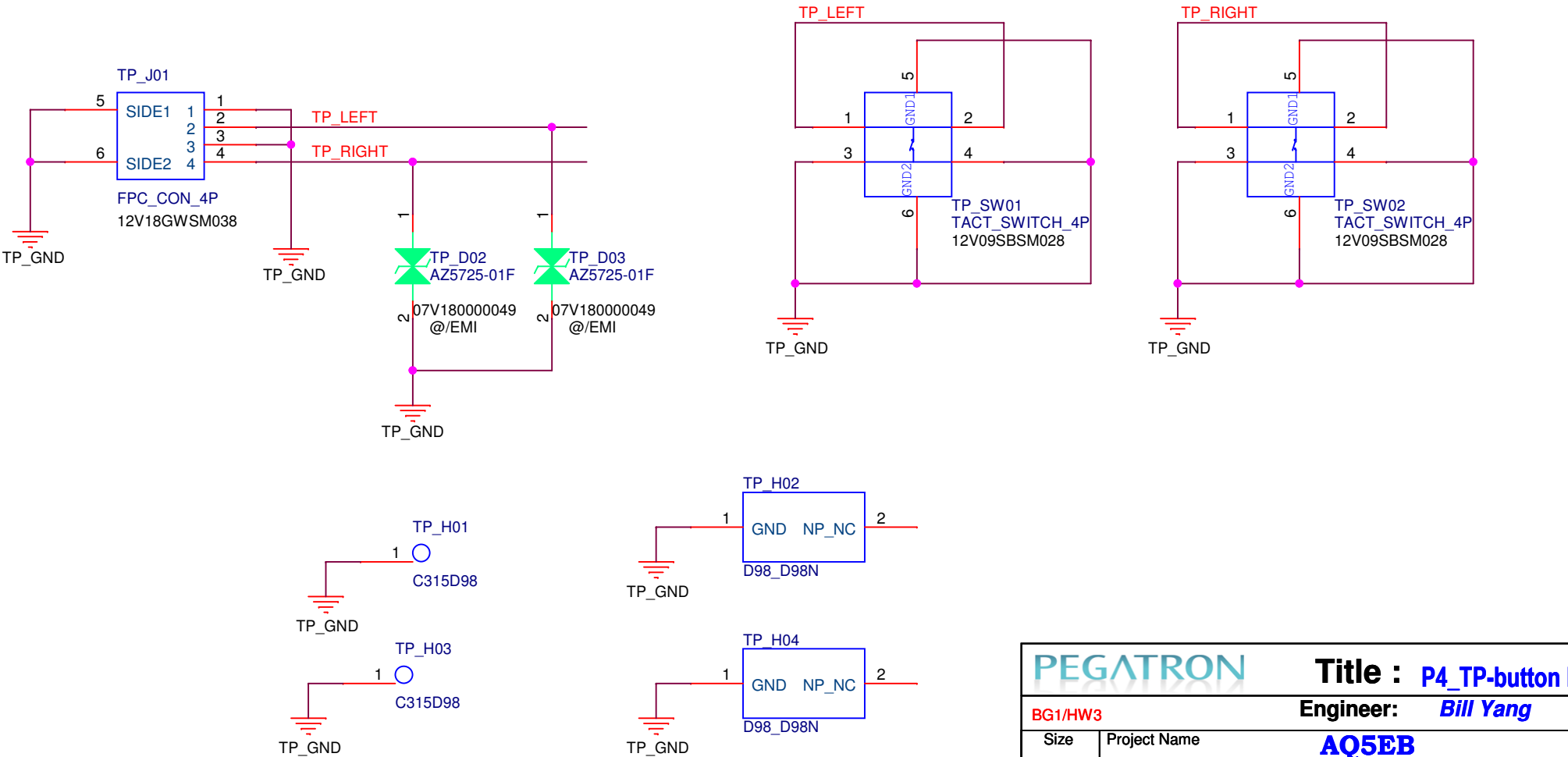


# P4\_LED BRD



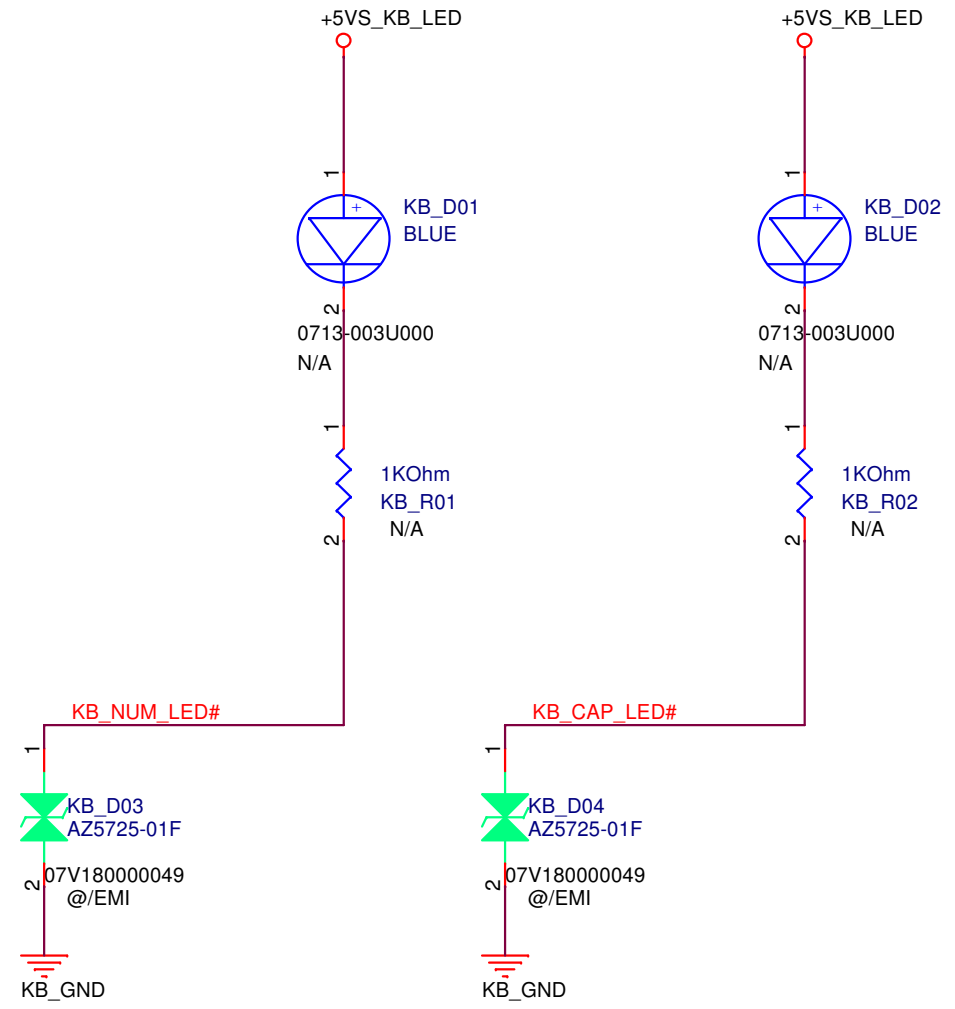
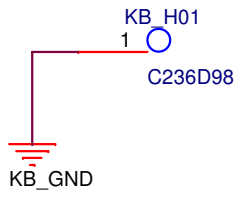
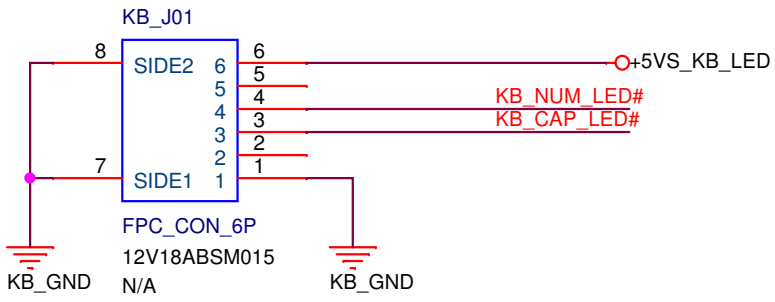
# P4\_TP-button BRD

## TP\_BRD to TP\_Model



PEGATRON		Title : P4_TP-button BRD	
BG1/HW3		Engineer: Bill Yang	
Size	Project Name		Rev
Custom	AQ5EB		
	P/N		
Date: Wednesday, August 23, 2017		Sheet	105 of 110





<b>PEGATRON</b>		Title : <b>P4_KB LED</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <b>Bill Yang</b>	
Size	Project Name		Rev
Custom	<b>AQ5EB</b>		1.1
Date: <b>Wednesday, August 23, 2017</b>		Sheet <b>106</b> of <b>108</b>	